Onchip digital calibrated 2mW 12b SAR ADC with reduced input capacitance

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Abstract

We present a 12-bits asynchronous SAR ADC with a low complexity digital onchip calibration and just 2pF of total array capacitance. The ADC architecture utilizes a redundant weighting switching of 4fF MOM capacitors consuming 14 clock-cycles to complete the conversion. Taking advantage of redundancy, the weights of the MSB capacitors are estimated using the LSB array, thus it is possible to digitally compensate for the mismatch nonlinearity directly over the ADC output. The circuit consumes 2mW on a core area of 300umX500um in 180nm CMOS technology. ENOB of 11.5-bits was post-layout simulated after calibration. Sample characterization is ongoing.

Onchip Calibration

Mismatch calibration is a better solution for high-resolution SAR ADC, then chip-by-chip calibration is not necessary, which will reduce the testing costs. Calibration techniques with bearable complexity and small area performed during the system startup, without external components or signals, is an attractive strategy for the new generation of ASICs for HEP. Mismatch compensating allows us to reduce the array capacitor unit close to the limit imposed by kT/C noise and thereby leading to considerable energy and area reduction. Minimizing the total capacitance of the SAR ADC will relax the speed requirement of the voltage reference buffer and the input signal driver (analog Front-end output), which are commonly power-hungry blocks.

ADC features

♣ 2 bits of redundancy. More robust against conversion errors. 14 clock cycles to complete the conversion. The digital part decodes 14 bits to 12 bits (see Fig 1).

♣ Onchip comparator offset calibration (6 bits) before capacitor mismatch calibration (Fig. 2). The offset trimming provides a 20 mV tuning range with 1.25 mV of resolution.

♣ New technique for MSB capacitors (C_{i+1} to C_{13}) mismatch calibration using the LSB capacitors (C_0 to C_i) based on an improved approach from [1]. LSB capacitors are utilized to extract the real weights of the MSB capacitors. 3-σ estimated DNL caused by LSB capacitor is within 1 LSB, thus these not need to be calibrated. Calibration algorithm is illustrated in Fig.3. Knowing the real weights of the MSB capacitors, the digital output can be digitally decoded improving the linearity.

♣ The capacitive DAC is implemented for a 4fF MOM capacitors array. The MOM cell structure is shown in Fig. 4. The total input capacitance is only 2pF.

♣ It employs top plate sampling and monotonic switching [2] for half of the unit capacitors because the procedure has 14 decision steps but only 13 C-DAC actions.

♣ $1/2V_{REF}$ is used for the LSB capacitor reference voltage in order to reduce the MSB capacitor size by 1/2.

12-bit SAR ADC architecture

Fig. 1

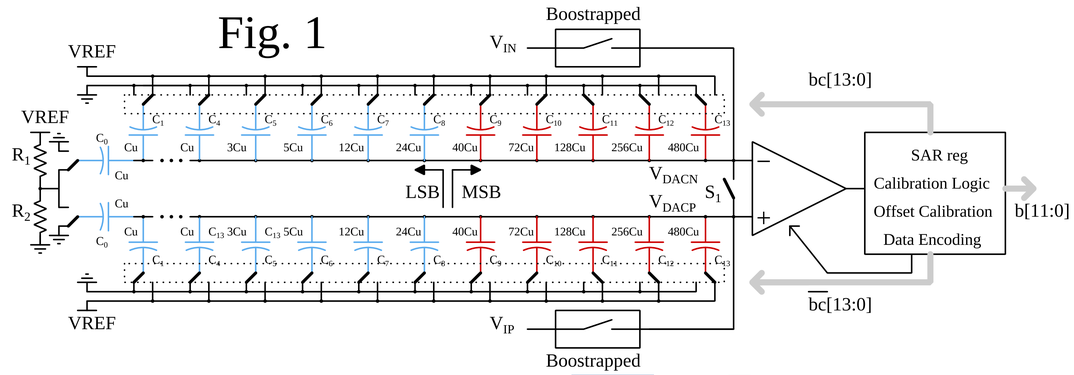


Fig. 2

Fig. 3

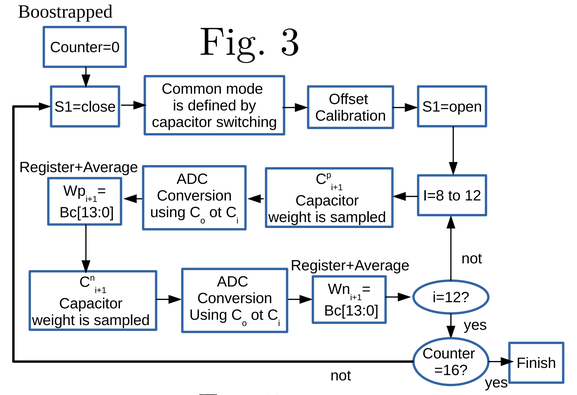


Fig. 4

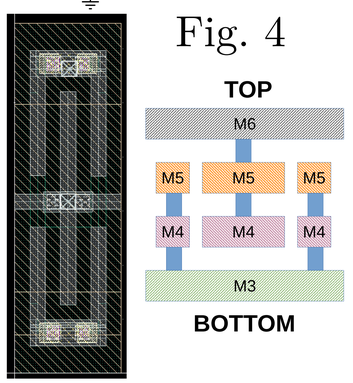
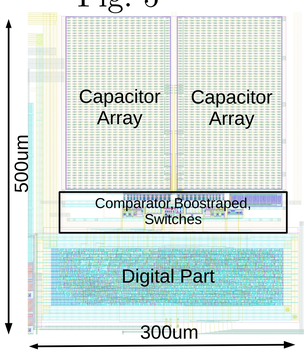


Fig. 5



References

References

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