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Onchip digital calibrated 2mW 12b SAR ADC with reduced input capacitance

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We present a 12-bits asynchronous SAR ADC with a low complexity digital on-chip calibration and just 2pF of total array capacitance. The ADC architecture utilizes a redundant weighting switching of 4fF MOM capacitors consuming 14 clock-cycles to complete the conversion. Taking advantage of redundancy, the weights of the MSB capacitors are estimated using the LSB array, thus it is possible to digitally compensate for the mismatch non-linearity directly over the ADC output. The circuit consumes 2mW on a core area of 300um x 500um in 180nm CMOS technology. ENOB of 11.5-bits was post-layout simulated after calibration. Sample characterization is ongoing.

Summary (500 words)

The growing HEP experimental needs are pushing for improved acquisition systems where ADCs with increased resolution are desired, going even beyond 12 bits, with sampling frequencies in the order of tens of MHz. Small area and power consumption are critical specifications since many channels in a single integrated circuit are a trend in HEP detectors. Successive Approximation Register (SAR) has been shown in the last decade to be an adequate architecture to reach these specifications, but for resolutions greater than 10 bits the capacitive array mismatch limits the effective resolution. Using special techniques for the capacitor array layout and increasing the unit capacitor are strategies often used by the designer to reduce the mismatch, but this generally leads to an excessive increase in power and area consumption. Mismatch calibration is a better solution for high-resolution SAR ADC, then chip-by-chip calibration is not necessary, which will reduce the testing costs. Calibration techniques with bearable complexity and small area performed during the system startup, without external components or signals, is an attractive strategy for the new generation of ASICs for HEP. Mismatch compensating allows us to reduce the array capacitor unit close to the limit imposed by kT/C noise and thereby leading to considerable energy and area reduction. Minimizing the total capacitance of the SAR ADC will relax the speed requirement of the voltage reference buffer and the input signal driver (analog Front-end output), which are commonly power-hungry blocks. In multi-channel ASIC where many ADC instances are integrated in a single chip, many bond-pads and large decoupling capacitance are required for the voltage reference due to the settling error generated by the bondwire inductance during the bit cycling phase. This effect becomes really critical as the sampling frequency increases. Redundant weighting is a simple way to avoid the conversion errors generated by this, with the cost of consuming more clock cycles to complete the conversion. This work presents the design of a 25MHz 12-bits asynchronous SAR ADC with redundant weighting switching of MOM capacitors in 180nm CMOS technology. The total array capacitance is only 2 pF and the whole ADC consumes less than 2mW on a core area of 300 um X 500 um. A new on-chip digital calibration approach that just lasts some microseconds during the chip start-up is presented. The post-layout simulation results show an ENOB of 11.5 bits after calibration. The chip is being produced and experimental results will be available soon.

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