A Four-Channels Front End Electronics for ATLAS Muon-Drift-Tubes Detectors in 65nm CMOS Technology

S.A.A.Shah, M.De Matteis, A.Baschirotto
University of Milan-Bicocca, Milan, Italy
R.Richter , H.Kroha, M.Fras,
Max-Planck-Institut for Physics, Munich, Germany

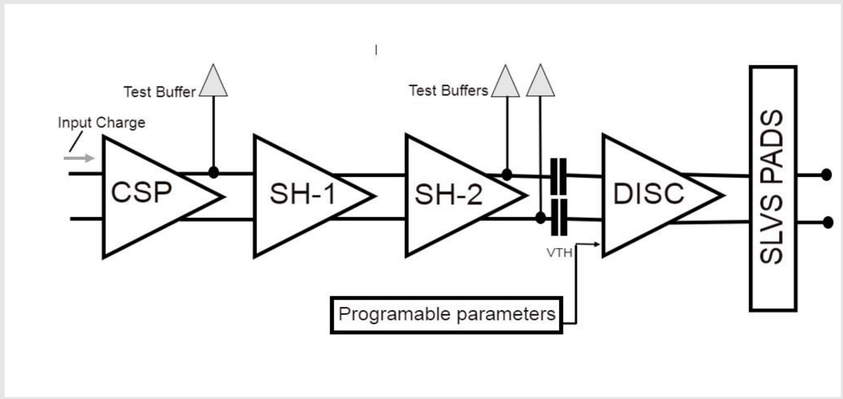
Introduction

- ATLAS experiment designed to explore the proton-proton collisions at the CERN
- Ionizing track crossing a MDT tube generates a string of electrons which drift towards the anode wire
- The MDT chamber design is optimized for precision tracking
- AFE Electronics detect arrival of charge and give information regarding Charge arrival time and amount of charge
- Higher speed (for higher instantaneous luminosity), lower area, robust Front-End Electronics are needed

Novelty In Design

- This AFE Design is a new, advance version of a CHIP, designed in 130nm CMOS process, being used in ATLAS experiment
- Scaling down the technology to 65nm CMOS process
- Operating at Low Supply Voltage of 1.2V
- Minimum and Simplified Architecture
  - Two Stage Shaper
  - No Pre-Discriminator Stage
  - Single Mode of operation (ToT Mode)
- Improving Passive elements sizing
  - Targeting Area Efficient Design
- Replacing LVDS by SLVS pads
  - Power Efficient, High Speed
- New Block of PISO-SIPO to confirm the correctness of Digital contents for Chip operation
- Variable Dead Time up to 500ns with a step of 30ns

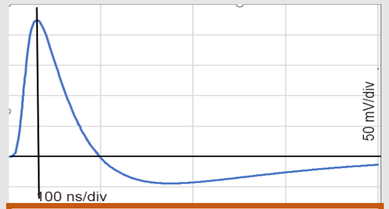
Functional diagram of the ASD using bipolar shaping



- Charge Sensing Preamplifier (CSP)->DA1->DA2->DA3(three shaping stages) -> discriminator -> SLVS PADS
- The Design area is 2×2=4 mm2

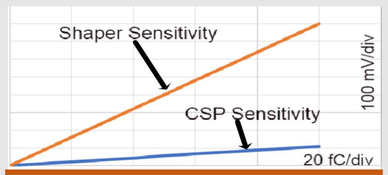
Methodology

- CSP, first stage of Design, performs charge to Voltage conversion
- A 2-Stage Single Ended amplifier topology is used for this stage
- Amplifier of Bandwidth of 2.4Hz is designed for Fast Peeking time
- Peaking Time of CSP is 11ns
- High Transconductance of 25mA/V is set, targeting minimum noise
- Input noise density of CSP is 1.1 nV/√Hz
- Linear sensitivity of 1.1mV/fC for 5-100fC range
- SNR at CSP output is 14.5 dB



Signal peaking time of 14.6 ns with 60 pF detector capacitance

- 2 Stage Shaper is designed to Implement Bipolar Scheme
- Implementing Two Poles
  - FP1=1.55MHz & FP2=1.41MHz
- Implementing Two Zeroes
  - FZ1=0.77MHz & FZ2=0.365MHz
- Pass Band gain of Shaper 17.6 dB
- Linear sensitivity of 8mV/fC for 5-100fC range



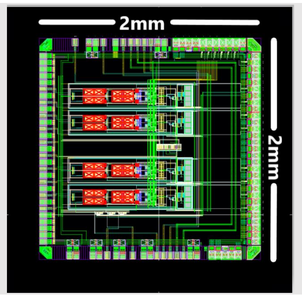
Sensitivity of CSP and Shaper is 1.1mV/fC and 8mV/fC respectively

- Uncompensated 2 Stage OP Amp used for Discriminator
- To set threshold Voltage, two 8-Bit String DACs are used
- A variable threshold of up to 256mV can be set with LSB of 2mV
- SLVS PADS are used to convert signal to external low-level signal
- Voltage swing of 200 mV on a 100 Ω load
- Common Mode voltage of 200 mV

Design Specification

Parameters	Values (This Work)	Values ASD 130nm
CMOS Technology	65nm	130nm
Total Area	4mm^2	7.638mm^2
Supply Voltage	1.2V	3.3V
Channel Power	16mW	33mW
Detector Parasitic Cap	60pF	60pF
Shaping Function	Bipolar	Bipolar
Shaper Stages	Two	Three
Input Charge	5—100fC	5—100fC
Signal Peaking Time	14.6ns	15ns
Front End Sensitivity	8mV/fC	14mV/fC
Input noise density	1.1 nV/√Hz	1.3 nV/√Hz
SNR at Min Input Charge	15 dB	15 dB

Chip Layout



Signal Response