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DIAMASIC: A multichannel front-end electronics for high-accuracy time measurements for diamond detectors

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This paper describes the design and testing results of an 8 channels preamplifier-discriminator circuit based on a resistive feedback Transimpedance Amplifier architecture and a Leading-Edge Discriminator stage for fast high-accuracy time measurement systems. The circuit has been designed in a 130 nm CMOS technology. It is intended to be used as a Front-End-Electronics for measuring the Time Of Flight using diamond detectors. The size of the chip is 1.27x1.22mm² and the total power consumption of one channel is 1.5mW with a power supply of 1.2V. Testing results shows a timing jitter of about 80ps for a 10fC input charge pulse.

Summary (500 words)

Recently, Chemical Vapor Deposition (CVD) Diamond detector offers an attractive alternative to silicon detector due to its outstanding performances such as the higher charge mobility (2200cm2/Vs and 1600cm2/Vs for electron and hole respectively), low leakage current (high bandgap of 5.45eV) and radiation hardness capabilities. This type of diamond detectors is used as solid-state ionization chambers: it means that the detector can be modeled as a current source with both a capacitor and a resistor in parallel of each other. The resistor is neglected because it is so high to be considered (several Tera Ohms). The goal of this project is to measure the Time Of Flight (TOF) of particles with a resolution of tens of picosecond using CVD double-side stripped metallized diamond detector. This leads to some challenges in the design of the dedicated Front-End readout Electronics (FEE): large bandwidth and low noise. The proposed circuit is an 8 channels preamplifier-discriminator circuit based on a resistive feedback Transimpedance Amplifier (TIA) architecture and a Leading-Edge Discriminator stage. The TIA is sized using the gm over id methodology which is suitable for low power applications. In our case, the timing resolution of the system is estimated as the quadratic sum of three main parameters: The Time-To-Digital Converter (TDC) resolution that is related to its topology, the time walk of the discriminator stage which appears when signals with same rise time but different amplitude are detected, and the timing jitter of the front-end stage. It was already shown that the time walk can be corrected using post-processing techniques as the time over threshold method or the constant fraction discrimination method. The timing jitter of the front-end stage depends on both the bandwidth and the noise of the amplifier stage. It is deemed to be the most critical parameter which needs to be reduced in order to guarantee the best timing resolution. Thus, during this study, the timing jitter error is considered as the criteria of time resolution. For this, a more accurate model of the circuit is proposed adding the interconnection inductances of bonding wires between the detector and the FEE. We developed as well a new mathematical model of the timing jitter capable of obtaining the optimum values of the input impedance and the bandwidth. The model is implemented in MATLAB Simulink and compared to electrical simulations and testing results to demonstrates the accuracy of the new design approach and the timing jitter estimation equation. Using the proposed methodology, we could achieve a measured timing resolution of about 80ps with an input charge pulse of 10fC and a total power consumption of only 1.5mW for a single channel.

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