A low power clock generator 400-1800 MHz for ADPLL

E. Atkin*, P. Ivanov, D. Normanov

National Research Nuclear University MEPhI (Moscow Engineering Physics Institute)

There is a trend in readout electronics to digitize signals early on. That results in the development of predominantly front-end mixed-mode (analog-to-digital) ASICs. The digital part of these chips needs phase-locked-loop block (PLL). The most of critical part of PLL is the clock generator (CG). CG must be low-power, area-efficient, work stably at a wide range of supply voltage and temperature.

The paper presents a low-power all-digital clock generator (ADCG) designed as a key part of phase locked loop block. The clock generator operates with a reference clock frequency of 10 MHz to 50 MHz and generates an output signal ranging from 400 MHz to 1800 MHz in 10 MHz steps.

ADCG design

The block diagram of the ADCG is shown in Figure 1. It contains the following units: a counter, an oscillator controlled by a digital code, frequency divider and control one.

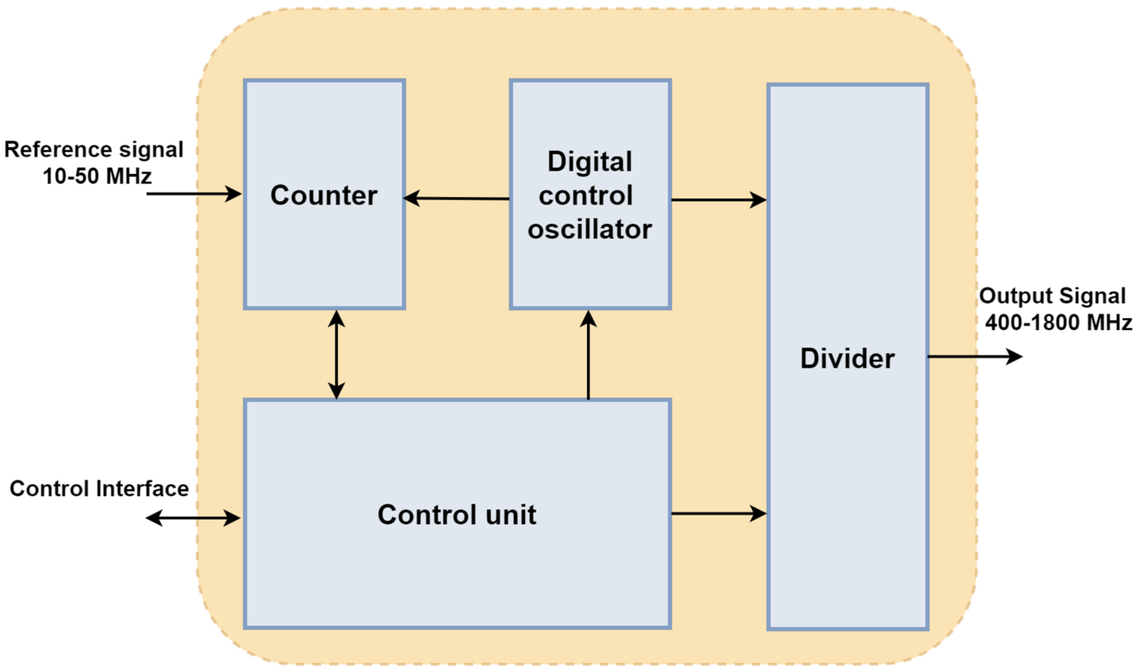

Figure 1. ADCG block diagram

The ADCG operation principle is based on counting the number of clock pulses at the output of the oscillator in a given time window and comparing it with the calculated theoretical value. The control unit compares the calculated and actual counter values and generates code for digitally controlled oscillator. The oscillator unit is a ring generator on NAND gates. It contains two segments for coarse and fine frequency tuning.

Fine tuning is shown in Figure 2. It is based on switching the gate inputs. The precision of the tuning is defined by a small difference in the signal propagation delay for different inputs. Coarse one is shown in Figure 3. It is based on the activation or deactivation of a certain number of gates in the generator loop.

This approach allows to regulate the frequency of the oscillator with a very small time step and ensure high accuracy and stability of the generated frequency.

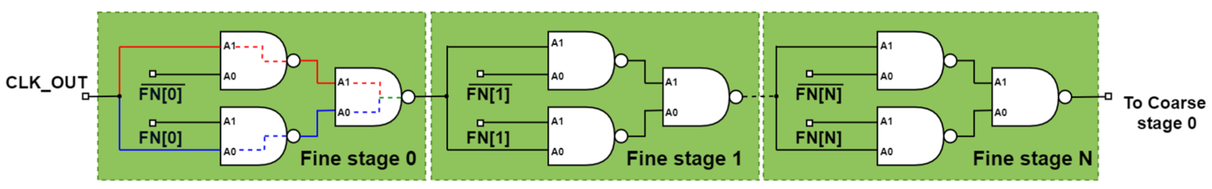

Figure 2. Fine tuning

* Correspondent e-mail and phone: evatkin@mephi.ru +7 499 324-25-97

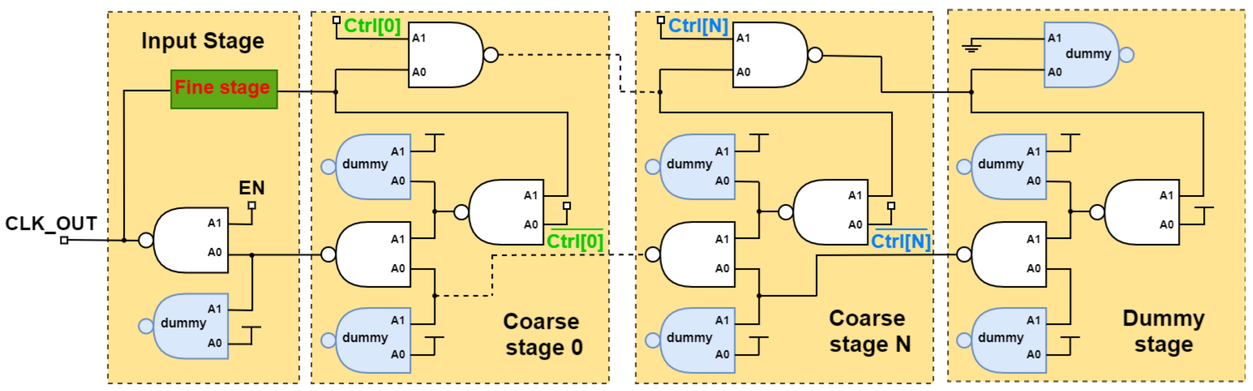

Figure 3. Coarse tuning

Finite-state machine diagram of the control unit is presented in figure 4. It includes 4 states:

1) IDLE state − Block is inactive;
2) Coarse tuning stage (GNT0) − The number of active links is calculated based on the average delay of one link in the chain;
3) Fine tuning stage (GNT1) − +1 active link in the chain;
4) Fine tuning stage (GNT2) − -1 active link in the chain.

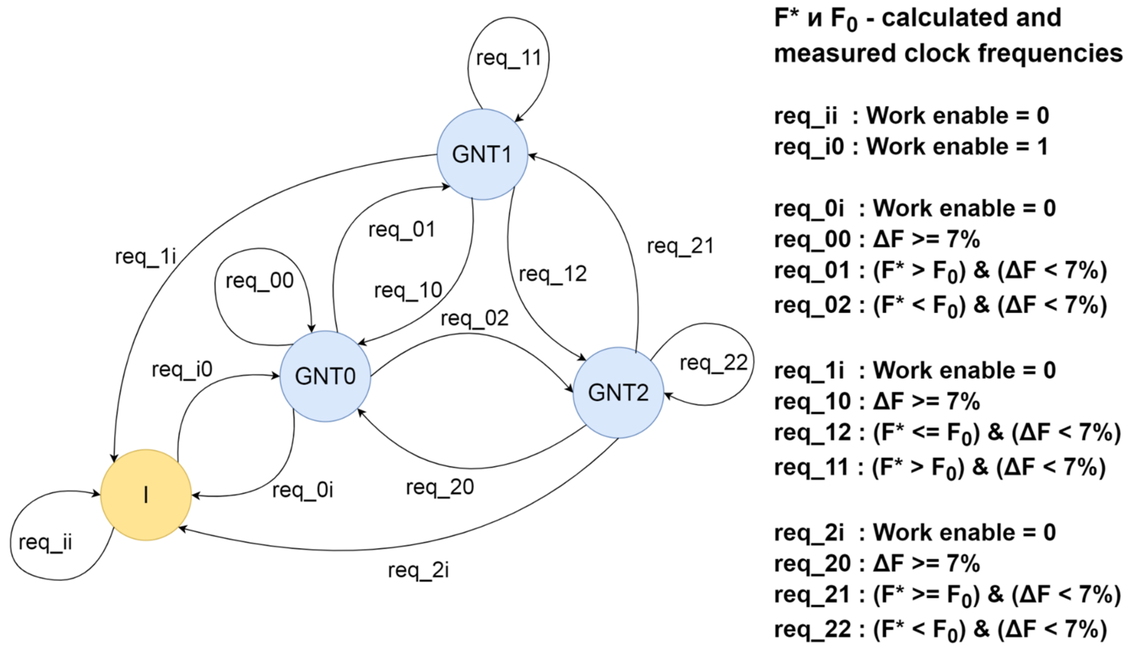

Figure 4. Finite-state machine diagram of the control unit

The ADCG has been prototyped in the TSMC 28 nm technology (Figure 5). The power consumption and chip area of the block are 1.5 mW and 80 x 80 μm^2 correspondingly. The measured block jitter is 20 ps.

The first application of ADCG is planned to be used as a part of a phase-locked loop for a data concentrator ASIC [1] intended for a time-projection chamber of Multi Purpose Detector at NICA, Dubna.

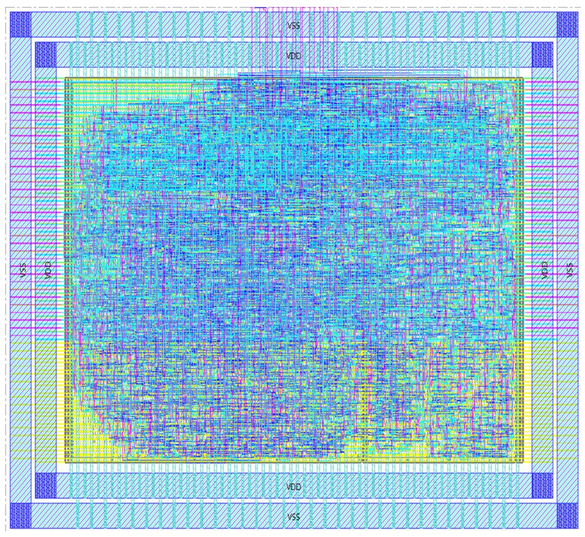

Figure 5. ADCG layout

Conclusion

The ADCG block has been designed as a symbiosis of known solutions [2-4] and prototyped in 28 nm CMOS process. It generates clock signals in the frequency range from 400 MHz to 1800 MHz in 10 MHz steps.

Acknowledgement

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Reference

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