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A low power clock generator 400-1800 MHz for ADPLL

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This paper describes a low-power all-digital clock generator (ADCG) designed for reading and processing signals from detectors of large physical experiments. The clock generator operates with a reference clock frequency of 10 MHz to 50 MHz and generates an output signal ranging from 400 MHz to 1800 MHz in 10 MHz steps. The clock generator has been approved in 28nm CMOS technology of TSMC. The power consumption and chip area of the block are 1.5 mW and 80x80 m^2 correspondingly. A wide range of reference and output frequencies makes this block versatile in application.

Summary (500 words)

There is a trend in modern electronics to digitize signals early on. This trend is leading to the development of predominantly analog-to-digital ASICs for physical electronics. The digital part of these ASICs needs phase-locked-loop block (PLL). The most of critical part of PLL is the clock generator (CG) block. CG block must be low-power, area-efficient, work stably when the supply voltage and temperature change in a wide range. CG block described in this article is fully digital (ADCG) and is designed to be used as a universal block for reading and processing signals from detectors of physical electronics. The block diagram of the ADCG block is shown in Figure 1. The ADCG contains the following blocks: a counter, an oscillator controlled by a digital code, a frequency divider and a control unit. The range of reference frequencies at which the ADCG operates varies from 10 to 50 MHz in 10 MHz steps. At the output, the ADCG generates signals in the frequency range from 400 MHz to 1800 MHz in 10 MHz steps. The ADCG principle of operation is based on counting the number of clock pulses at the output of the oscillator in a given time window and comparing it with the calculated theoretical value. The control module compares the calculated and actual counter values and generates an oscillator frequency control code. The oscillator block is a ring generator on NAND elements. It contains two segments - coarse and fine frequency parts. Coarse frequency adjustment is based on the activation or deactivation of a certain number of NAND gates in the generator loop. Fine tuning is shown in Figure 2 by switching the inputs of the NAND gate and is based on the difference in the signal propagation delay for different inputs of the NAND gate, which is very small. This approach allows to regulate the frequency of the oscillator with a very small time step and ensure high accuracy and stability of the generated frequency. The ADCG block has been tested in TSMC 28 nm technology using CAD Cadence. The power consumption and chip area of the block are 1.5 mW and 80 x 80 μm2 correspondingly. The measured block jitter is 20 ps. The ADCG is planned to be used as a part of a phase-locked loop for a data acquisition microcircuit for a time-projection camera of a multipurpose detector (MPD, Dubna).

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