Verification of ATLAS detector readout with FPGA-based front-end emulator

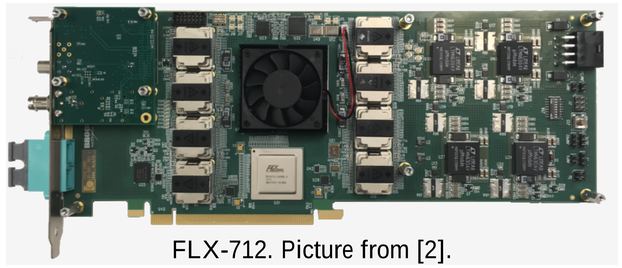
R. Luz[1] on behalf of ATLAS TDAQ Collaboration

[1]Argonne National Laboratory, 9700 S Cass Ave, Lemont, IL 60439, USA

Motivation

- FELIX is an FPGA-based data router being developed as part of the ongoing upgrade of the ATLAS experiment.
- FELIX relies on synchronous data aggregation protocols like GBT and lpGBT [4].
- FELIG was created to facilitate validation and benchmarking of FELIX.

Hardware platform



FLX-712. Picture from [2].

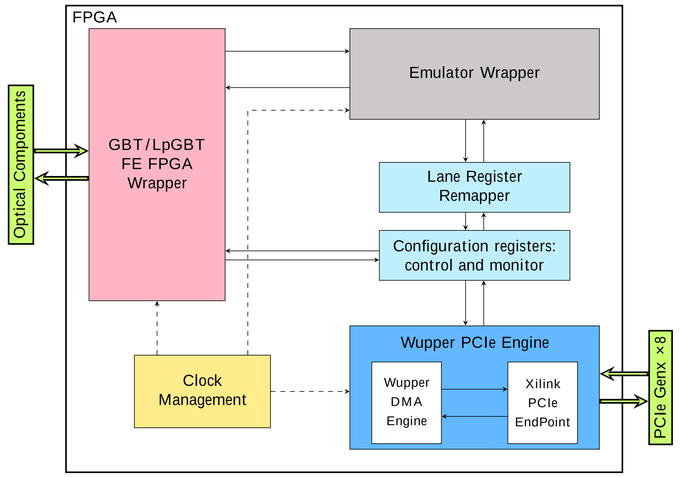
- FELIG was first implemented in the HTG-710 board.
- FELIG was recently ported to the largely available FLX-712 card, the current FELIX hardware platform:
  - Based on a Kintex UltraScale XCKU115 FPGA,
  - Supports 48 high-speed optical links via minipods,
  - Two jitter cleaners, making clock recovery for FELIG much easier than before.
- The recommended FELIG server includes two FLX-712:
  - One for FELIG and the other for FELIX, connected using the optical fibers,
  - A TTC system can be connected to FELIX, and its signals redirected to FELIG.

References

[1] ATLAS Collaboration, The ATLAS Experiment at the CERN Large Hadron Collider, JINST 2008
[2] ATLAS FELIX Group, FELIX User Manual
[3] Abulaiti et al., Manual of the front-end emulator for FELIX (FELIG), ATL-COM-DAQ-2021-009
[4] GBT/lpGBT team, GBTX Manual and lpGBT Manual
[5] C. A. Gottardo, FELIX and SW ROD Commissioning of the New ATLAS Readout System, IEEE NSS/MIC, 2020

Firmware

- The GBT/lpGBT link wrapper, registers and Wupper PCIe engine are copied from the FELIX firmware.
- A data emulator was developed, responsible for:
  - Generation trigger management: External via TTC system or internal counter,
  - Data encoding: See data formats panel,
  - GBT/lpGBT frames creation: Allows for a maximum of 32-bit E-group widths.
- Clock management: Local clock responsible for slow control and internal trigger generation. RX recovered clock drives the TX channels.



FELIG firmware block diagram. From [3].

Data formats

- Current emulated data is based on a countdown state machine. More realistic generators can be easily plugged-in.
- GBT and lpGBT protocols are implemented, including both FEC codes and data rates used in lpGBT.
- 2, 4, 8, 16, and 32-bit E-Groups widths are allowed as well as MSB or LSB first.
- Direct, 8b/10b and 64b/66b data modes are available.

Software

- FELIG uses FELIX's software tools, namely for card initialization and registers programming.
- A set of commands, felig-tools, were created to facilitate FELIG configuration and control.
- felig-tools is distributed with the FELIX software.

Selected validation results using FELIG

System performance at 100 kHz trigger rate (phase-1).

Stress test to evaluate performance for rates up to 1 MHz (phase-2).

Both plots from [5]

Summary

- FELIG is supported on the HTG-710 and the FLX-712.
- FELIG helped validate FELIX and was used to uncover a few bugs.
- Extensive hardware testing for lpGBT communication is planned.