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Hough-transform-based FPGA track processor for the ATLAS experiment at CERN

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The Hough-transform-based FPGA track processing is considered for the trigger system of the ATLAS detector at the Large Hadron Collider at CERN as a part of the upgrade for the High-Luminosity program. The prototype firmware has been developed to evaluate system size. The track processing is organized as a pipeline to increase data processing and clock rates. This Hough transform accumulator can use input pixel and strip hits, stubs, and space-points. It outputs track candidates for bins that meet the track reconstruction requirements. The accumulator is configurable with number of bins in φ and q/pT, and number of input hits.

Summary (500 words)

The ATLAS experiment at CERN will require identification of charged particle tracks for its trigger system. The trigger algorithms are executed using CPUs however, we are considering to offload track identification to FPGAs. To perform pattern match for track reconstruction we have prototyped firmware that uses two-dimensional Hough transform identification with q/pT and ϕ coordinates. The pattern reconstruction is targeting track candidates with pT>1 GeV and |d0|<2mm. Bin sizes of the Hough transform accumulator are driven by the random scattering and the impact parameter range. The prototype firmware has been configured to fit Xilinx Alveo U250 board to evaluate the system size.

The hough transform accumulator firmware operates as a pipeline. Event data are divided into regions and regions are processed separately. Each region corresponds to a slice in η-z0 phase-space to reduce occupancy of the accumulator. Resolution of the ITk hits and space-points is reduced to match the accumulator bins and the full resolution hits and space-points are stored in a buffer. The accumulator cells are loaded with pointers to the buffer and ITk layer information. Once loading is complete, selected cells with appropriate layer patterns are readout for further processing and the pointers are used to lookup the original hits and space-points. The accumulator firmware is configurable with numbers of bin, number input hits, and layer patterns. An accumulator with 256 bins in ϕ, 200 bins in q/pT, 16 hits per cell, and 1023 hit buffer takes about 50% of U250 LUTs. It uses fewer FFs and DPSs. We are exploring ways to reduce the FPGA resource utilization and proximity-based removal of duplicate track candidates.

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