Versatile free-running ADC-based data acquisition system for particle detectors

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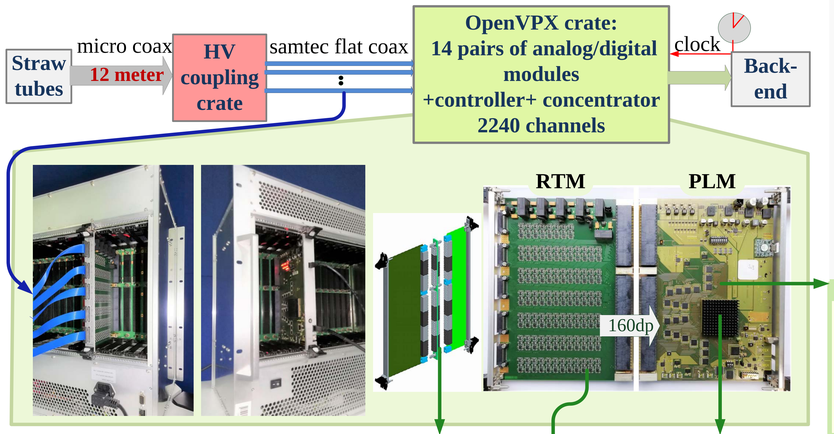
A high density data acquisition system integrating over 2000 channels inside of a single OpenVPX crate is intended to be used in different applications, e.g., gaseous or scintillator-based particle detectors. 14 payload slots, controller and data concentrator communicate one with other via multi-gigabit backplane. Each payload slot consists of a front module for digital and a rear transition module for analog processing. This single pair implements 160 full chains including amplification/ shaping, sampling, and feature extraction. Sampling rate and ADC resolution are configurable for 80-1000 MS/s, 8-14 bit. The system has been tested at COSY at Jülich Research Center (Germany).

System Structure with Off-Detector Front-end



Why Off-Detector Front-end?

1. No mechanical and heating elements inside/around of detector
2. All sensors data are the same time at the same place
   → time sorting/clustering takes place at a very first stage, trigger/veto/coincidence implementation is facilitated
3. Well suitable for clock skew adjustment and set-up support

Drawback of a long cabling:

- Cabling capacitance makes it ***impossible to get benefit of high sampling rates***
- Noise is higher, nevertheless acceptable if it does not appear as a greatest error contribution

Why Wave Form Sampling (WFS) ?

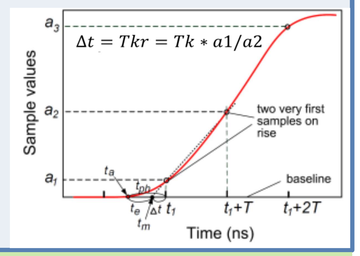
Time over threshold, time-to-digital converters are low power and low cost methods. Main lack: complicated pile-up reconstruction leading to a count rate loss. Low count rates are inherent also to time stretching methods and dSIPM due to long validation and readout time. ***WFS reduces the detector dead time down to pulse rise duration (~30 ns) .***

However, fast flash ADCS are power and cost expensive

High timing resolution with moderate sampling rate needed!

Pipelined ADCs (< 250 MS/s), keep a balance of a required timing resolution with low cost and power consumption

Non-Linear Rise Approximation (NLRA) [1] → the resolution is 1/100 of sampling period → calculates the pulse arrival time via the ratio of two very first samples on the rise



40x 4-channel HMCAD1520 ADCs

- Various modes, sampling rate vs. output bits and channel number
- Serial output data lines (2x12 bit/ch) up to 1 Gb/s
- Gain settings and a very low power consumption ~ 125 mW/ch.

Number of bits	Single Channel High Speed [MSPS]	Dual Channel High Speed [MSPS]	Quad Channel High Speed [MSPS]
8	1000	500	250
12	660	330	165
14	560	280	140

Adjusted OpenVPX backplane

- OpenVPX crate with VITA65 BackPlane (BP) from ELMA
- 14 payload and 2 management slots
- Analog and digital modules plugged from both sides of the crate: analog as Rear Transition Module (RTM), digital PayLoad Module (PLM) as a front board
- BP connects a RTM to its adjacent PLM with 160 diff. pairs. To get it, expansion plane of BP was modified

160 analog channels per RTM

- Low noise transimpedance amplifier (OPA874), gain of 400
- Shaping with the CR-RC² circuit
- Front-end electronics including cabling results in approximately 20-ns signal peaking time
- Built with discrete electronics. The configuration (BW, gain...) is currently possible via different RC components. ***The system could benefit if multichannel configurable integrated solution is used.***

DAQ throughput

Uplinks:

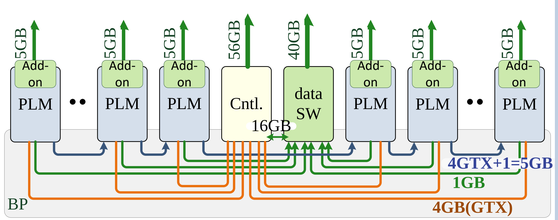
- USB3.0;
- 4 SFP+ are foreseen at PLM add-on board, each supports 10 Gb/s, total 5 GB/s

Configurations:

- Star, chain or mixed mode data transfer
- With or without controller and data switch if one of PLMs is configured as master

Backplane data:

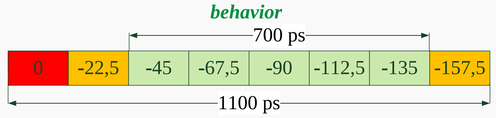
- GTX (10 Gb/s) and 1 Gb/s data lines
- Diff. and single ended GPIO for diverse triggers and others
- BP specified from ELMA: at least 10 Gb/s for the longest path



Single Virtex FPGA XCV585T, data capture

- ADC-to-FPGA lines tolerance (10 mm) corresponds to propagation difference of ~ 40 ps
- Zero Delay Buffers (ZDB) with channel-to-channel skew ~ 35 ps and clock jitter of a few ps
  → Channel-to-channel time skew is < 100 ps, thus no individual FPGA input delay tabs settings are needed. Channels are captured with the same clock phase set by MMCM
- With 150 MS/s, 2-lines LVDS transfer of 6 bits: 6x150=900 Gb/s, the stable data capture is ~ 700 ps
- ADC drive current set to 2.5 mA (default is 3.5 mA)

All three PLMs of the first design version show the same behavior



Test concept

ADC to FPGA data transfer: all ADCs send a **rump pattern**, 160 channels are tested at once and seen as single one

BW test with adapter and sinus generator:

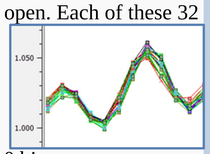
- 20 MHz

Quick test of full analog/sampling/processing chains:

One 1.5-m-long Samtec flat cable (contains 32 coax) is connected to RTM, the other end is open. Each of these 32 coax cables acts as antenna.

Signal deviations inside of band are small showing:

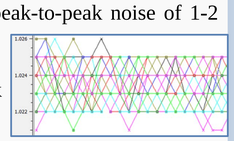
- Synchronous design
- Channel-to-channel difference < 10 bins



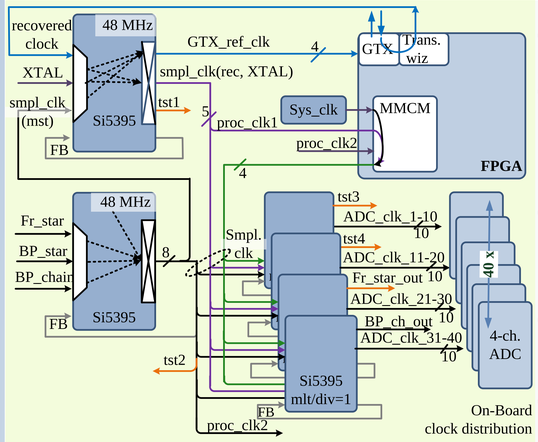
To check 160 chains, all five cables should be connected

Electronic noise

- RTM is not inserted, ADCs peak-to-peak noise of 1-2 bins
- RTM is inserted, Amplifier + ADC peak-to-peak noise of 4-5 bins
- 11 ADC bits are used

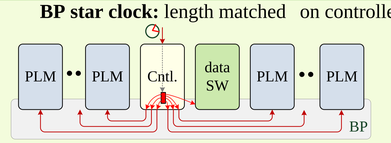


Clock distribution & Board synchronization

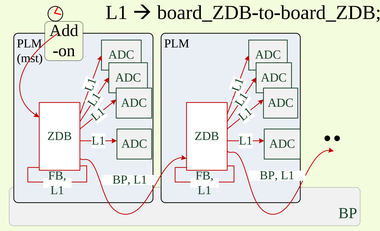


- All channels at PLM are fully synchronous, captured and processed as single one
- Synchronization via clock inputs: from Add-on board at front (Fr_star) BP star (BP_star) or chain clock (BP_chain), or free running from oscillator at PLM
- Mechanical clock switching will be replaced in the next PLM revision with clock buffers offering input multiplexing inside IC, as shown on the left
- Star clock configuration is preferable: not perfect Zero Delay is unimportant, because ADCs are at the same clock tree level
- Backplane clock star and chain configurations

BP star clock: length matched on controller



BP chain clock distribution: equal sampling phase via ZDB end equal length: L1 → ADC; L1 → ZDB-to-ZDB; L1 → FeedBack; L1 → board_ZDB-to-board_ZDB;



Implementation & results

NLRA, arrival time calculated via the ratio of two first samples on rise.

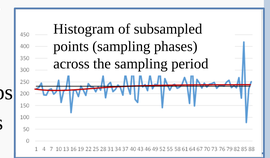
Xilinx® LogiCORE™ IP Divider Generator core based on LUTMult, 8-bit pipelined, **a single clock with o**ne DSP per channel.

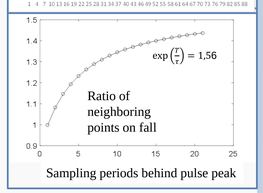
Our setup, 150 MS/s:

- Sampling phase error (SPE) ~200 ps
- Quantization error (ADC+ 8-bit divider) < 50 ps
- Noise contribution to timing error about 170 ps
- Arrival time resolution about 300 ps

Pile-up reconstruction:

- Via measured *an* and *an/an-1* on the pulse fall applying a lookup table of the ratio for the single pulse
- Resolution is lower than that for the first pulse: SPE ~400 ps, total ~460 ps





160 channels:

- arrival time
- pile-up reconstruction
- energy calculation

implemented on FPGA

Resource	Utilization	Available	Utilization %
LUT	99197	364200	27.24
LUTRAM	12320	111000	11.10
FF	108259	728400	14.86
BRAM	80	795	10.06
DSP	160	1260	12.70
IO	700	850	82.35
MMCM	1	18	5.56

Power consumption

Total power consumption per channel FPGA+ADCs+amplifiers: 50+125+100=~300mW

Summary & outlook

Ready and running since 2018:

- Two OpenVPX crates
- Three RTMs + three PLMs
- Data link USB 3.0

Tested OK:

- Amplifiers, shaping, sampling, FPGA data capture + processing
- NLRA: arrival timing method with resolution prooved via tracking
- Pile-up reconstruction
- 10 Gbits GTX links tested with IBERT (pins at Add-on board short-circuited for far-end loopback)

Next steps: Add-on board, next revision of PLM, controller

References

1. L. Jokhovets *et al.*, „Improved Rise Approximation Method for Pulse Arrival Timing“ IEEE transactions on nuclear science, vol. 66, no. 8, pp. 1942-1951, august 2019.

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