Contribution ID: **84** Type: **Poster**

Versatile free-running ADC-based data acquisition system for particle detectors

Tuesday 21 September 2021 17:29 (3 minutes)

A high density data acquisition system integrating over 2000 channels inside of a single OpenVPX crate is intended to be used in different applications e.g. gaseous or scintillator-based particle detectors. 14 payload slots, controller and data concentrator communicate one with other via multi-gigabit backplane. Each payload slot consists of a front module for digital and a rear transition module for analog processing. This single pair implements 160 full chains including amplification/shaping, sampling, and feature extraction. Sampling rate and ADC resolution are configurable for 80-1000 MS/s, 8-14 bit. The system has been tested at COSY at Jülich Research Center (Germany).

Summary (500 words)

In this work a configurable free-running data acquisition (DAQ) platform for large scale experiments is presented. This DAQ is intended to be used in different applications, such as gaseous detectors, neutron scattering experiments or PET-TOF detectors. The detector electronics consists of a number of sensors (photodetectors, straw tubes, etc.) coupled to the Nyquist filters, amplifiers, free-running ADCs, and a processing unit (FPGA) delivering events, energies and arrival time marks to a backend in real time. The DAQ is implemented inside of an OpenVPX crate. It includes all analog and digital processing stages and currently uses discrete electronics. However, increasing of the integration level is possible by step-by-step replacing of discrete components with ASICs.

There are 16 slots in the crate: 14 payload, one controller and one data concentrator slot. The slots are connected one with other via backplane with multi-gigabit bandwidth. The OpenVPX standard permits that modules can be plugged into the crate from both the rear and front sides. The backplane connects a module from rear side to its adjacent module on front side. This allows analog and digital processing units to be inserted from different sides. They can be developed and modified independently. The crate room is effectively used increasing the number of processing channels integrated in the crate. The analog unit includes 160 amplification/shaping channels and a row of Samtec connectors for sensor signals. The amplified/shaped signals pass through the backplane connector to the digital unit where 160 sampling channels and single processing FPGA are placed. Thus, one pair of modules provides 160 signal chains, and the whole single 19“-crate offers 2240 channels. It is foreseen, that data can be delivered to the backend system with bandwidth over 100 gigabits per second, and the system can be synchronized via such nets as White Rabbit or SODANET.

The high system flexibility relates to a wide range of sampling rates (from 80 up to 1000 MS/s). It is caused also by FPGA capability to implement different processing algorithms. In addition, the multi-gigabit backplane for data exchange between all slots benefits application specific functions, such as time sorting, cluster building, pre-tracking, and coincidence search. The number of processing channels is reduced at higher sampling rates (over 250 MS/s).

A proper choice of shaping parameters, sampling rate and timing algorithm results in a low power consumption of a single analog/sampling/processing chain (below 350 mW). Careful length-matched board routing and synchronization based on zero-delay clocks allow on-FPGA data capturing without individual channel setup delay. Thus, all channels are captured and processed as a single one.

The DAQ has been tested in the proton beam with gaseous particle detector –straw tube tracker at COSY (Cooler Synchrotron) at Jülich Research Center (Germany). The firmware for arrival timing, energy calculation and pile-up reconstruction as well as FPGA resource usage are also reported in this work.

Author: JOKHOVETS, Lioubov (Forschungszentrum Jülich GmbH)

Co-authors: Dr KULESSA, Pawel (Forschungszentrum Jülich, GSI Darmstadt); Mr ERVEN, Andreas (Forschungszentrum Jülich); GREWING, Christian (Forschungszentrum Jülich); HAHNRATHS VON DER GRACHT, Tanja (Forschungszentrum Jülich); HARFF, Markus (Forschungszentrum Jülich); Dr OHM, Henner (Forschungszentrum Jülich); Dr

PYSZ, Krzysztof (Institute of Nuclear Physics, Cracow); Prof. RITMAN, James (Forschungszentrum Jülich, GSI Darmstadt, Ruhr-Universität Bochum); ROTH, Christian (Forschungszentrum Jülich); SCHLÖSSER, Mario (Forschungszentrum Jülich); Dr SEFZICK, Thomas (Forschungszentrum Jülich); Dr SERDYUK, Valeriy (Forschungszentrum Jülich); Prof. VAN WAASEN, Stefan (Forschungszentrum Jülich); Dr WINTZ, Peter (Forschungszentrum Jülich)

Presenter: JOKHOVETS, Lioubov (Forschungszentrum Jülich GmbH)

Session Classification: Posters Programmable Logic, Design Tools and Methods

Track Classification: Programmable Logic, Design Tools and Methods