Firmware Architecture of the Back-End DAQ system for the CMS High Granularity Endcap Calorimeter detector

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The CMS High Granularity Calorimeter (HGCAL) [1]

The HGCAL detector (Fig. 1) is a high granularity 5-D (energy, x, y, z, t) imaging calorimeter that will replace the CMS endcap calorimeters in order to deal with the unprecedented radiation dose and the high pile-up challenges at High Luminosity - LHC.

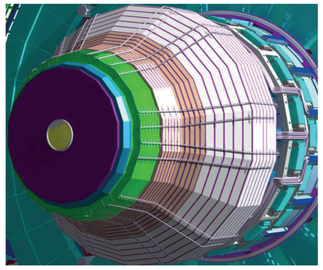

Figure 1. 3D drawing of one HGCAL installed on a CMS endcap.

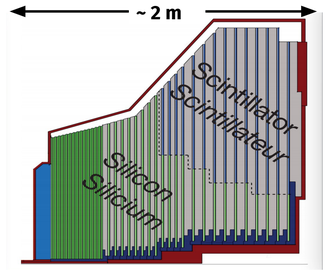

Figure 2. Side view of HGCAL showing the 50 detector layers (vertical strips).

Electromagnetic section (CE-E) :
- 28 layers of Silicon active elements (Fig. 2)
- Lead, Copper-Tungsten absorber.

Hadronic section (CE-H) :
- 22 Layers of Silicon and Scintillator active elements (Fig. 2).
- Stainless Steel absorber.

Key advantages :
- Good radiation tolerance.
- Fine granularity required for increased pile-up (up to 200 p-p collisions per event) during HL-LHC.

How will it work?

Incoming electrons, photons and hadrons produce "showers" of particles in dense metallic layers. These showers deposit energy and so generate signals in the silicon and scintillator detector layers, whose amplitudes are proportional to the original particle energy. The fine longitudinal (50 layers of detectors) and transverse (~0.5 - 1.0cm^2 cells) granularity results in extraordinary amounts of information about the structure of the showers, including their energies, positions and timing.

HGCAL will play a major role in maintaining the overall CMS Physics performance throughout the full HL-LHC period.

The HGCAL Control and Data Acquisition (DAQ) architecture

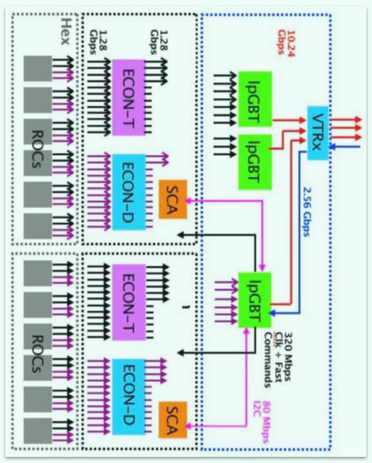

Figure 3. HGCAL detector read-out and control path.

Front-End (FE): The detector sensors information will be collected and digitised by custom rad-hard HGCAL Readout Chips (HGCROC) [2]. Data from multiple HGCROCs will be concentrated using dedicated concentrator ASICs (ECONs). The concentrated data will be sent to the Back-End via the radiation hard, low power lpGBT chipset through fibres (9k total) running at 10Gb/s (see Fig. 3). The lpGBT chipset will also receive and distribute clock, configuration and fast commands data from the Back-End through a downlink running at 2.5Gb/s.

Back-End (BE) DAQ: The Back-End DAQ boards (based on the "Serenity" platform developed by a collaboration within CMS [3]) receive detector data from the ECONs via 10Gb/s lpGBT links. The BE DAQ concentrates and forwards them to the Central DAQ via a number 25Gb/s SLINKs. It also provides the required buffering to avoid data loss due to rate fluctuations and a configurable lpGBT-to-SLINK mapping to mitigate the variations in rate/channel. The BE DAQ is also responsible for configuring the FE electronics and distributing the high precision clock and the trigger signals to the on-detector electronics.

Central DAQ: The central DAQ hardware (DTH board) [4] distributes clock signals, synchronization commands, Level-1 trigger, and slow control to BE DAQ. It also receives event fragments from the BE DAQ, and subsequently concentrates, buffers and transmits them to the data-to-surface network.

Firmware Architecture

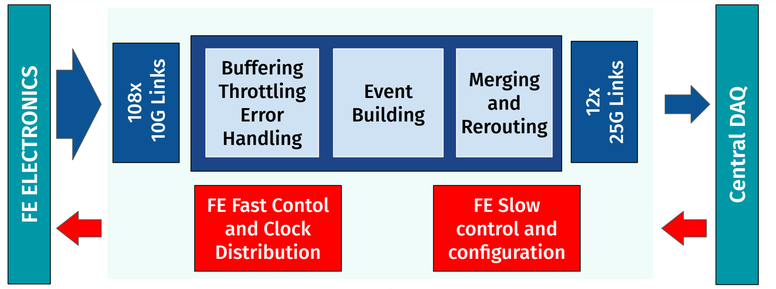

Figure 4. The Back-End DAQ firmware overview.

- ✓ Single firmware for all DAQ boards (Fig. 4).
- ✓ Flexibility to deal with all different Front-End flavours.
- ✓ Low routing congestion design.
- ✓ Configuration of the FE electronics
- ✓ Fast commands distribution to the Front-End electronics.
- ✓ Clock distribution.

Buffering : The FE-to-BE mapping varies significantly for the different parts of the HGCAL detector due to its geometry. A simplistic approach to deal with this issue could have been different firmware images for every BE DAQ board. Such approach could simplify the design(s) in the cost of significant maintenance complications. To avoid such a maintenance issue, a single firmware image architecture was chosen in which each Buffering block (processing unit) will always process data from 2 lpGBTs. There are 54 buffering blocks per FPGA, each receiving data from 2 lpGBT links and serving from 2 to 12 ECONDs, so each FPGA handles up to 108 lpGBT links. Data buffering, throttling and error handling mechanisms prevent data loss.

Event Building : Each processing unit reads out ECON data in a round robin fashion creating a larger Event frame. The event IDs and timing stamps of each incoming ECON are compared to local counters for synchronisation purposes.

Merging and routing : A configurable interconnect logic offers a flexible mapping of the 54 Event buffers to 12 fixed rate (25Gb/s) output links, in order to balance out the very inhomogeneous input rate (Fig. 5).

Slow Control : Dedicated blocks configure all the various FE ASICs via lpGBT and/or GBT-SCA ASICs, both in the higher (Silicon) and in the lower (Scintillator) radiation areas.

Fast Control : Dedicated blocks forward fast commands (e.g. L1A etc) to the FE ASICs. The generation of "local" fast commands (e.g resets) are also supported, a feature particularly important for the quick recovery of individual FE ASICs temporarily out of sync.

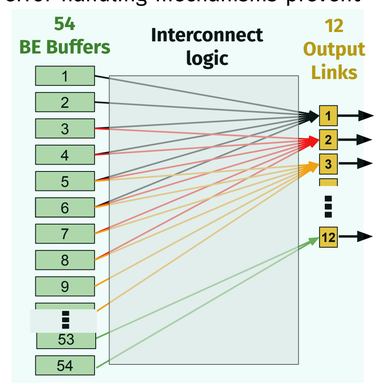

Figure 5. The partially programmable Input-to-output routing.

Firmware Status and Outlook

This firmware work is driving a full BE DAQ architecture review, improving upon the TDR expectations and towards pre-production in 2022. This was achieved thanks to the implementation & simulation strategies selected.

Implementation strategy: Special care has been taken during the firmware development to facilitate targeting different FPGA devices. Such approach was necessary for the selection of the optimum cost-efficient solution for the hardware.

Simulation strategy: A sophisticated testbench was designed to allow feeding realistic input data and comparing the firmware behaviour in respect with that of the system emulator (running in software), thus facilitating the validation of the firmware functionality.

Next steps: After careful studies, the best option seems to be a single-FPGA board equipped with a VU13P Xilinx Ultrascale+ FPGA serving 108 input links and 12 output links. The behaviour of the firmware must now be validated in the hardware, once the VU13P-based prototype will become available. In the meantime, hardware tests will take place using previous generation Serenity hardware.

References

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4. CMS Collaboration, The Phase-2 Upgrade of the CMS DAQ, Interim Technical Design Report, CERN-LHCC-2017-014, CMS-TDR-018, LINK

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