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Firmware Architecture of the back-end DAQ system for the CMS High Granularity Endcap Calorimeter detector.

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During the High-Luminosity phase of the LHC, the CMS endcap calorimeter will be replaced by the High-Granularity Calorimeter (HGCAL). A first firmware for the back-end DAQ system of the CMS Phase-2 upgrade HGCAL was implemented in the Serenity ATCA hardware. The system is responsible not only for the readout of the detector but also for its slow control and timing. To facilitate system maintenance, the firmware is optimized to handle all the different Front-End electronics configurations and data rates using a single —highly configurable —design. The architecture and implementation of the back-end DAQ system will be presented here.

Summary (500 words)

The next phase of the Large Hadron Collider (LHC), known as High Luminosity LHC (HL-LHC), will commence its operation in 2027. During this phase the HL-LHC is foreseen to provide about ten times the LHC dataset, operating at an instantaneous luminosity around five times higher than presently available. In order to cope with the new challenging conditions, the CMS collaboration will replace the existing electromagnetic and hadronic endcap calorimeters with the new High Granularity Calorimeter (HGCAL). The new detector will feature unprecedented transverse and longitudinal segmentation for both electromagnetic (CE-E) and hadronic (CE-H) compartments and will have the ability to withstand the high radiation levels. The CE-E and a large fraction of CE-H will use silicon hexagonal shaped detector modules as active detector material, while the lower-radiation part of the CE-H will be instrumented with scintillator tiles. A new read-out ASIC (HGCROC) was designed to meet the high dynamic range, low noise and high-precision timing information requirements of the detector. A concentrator ASIC (ECOND) will collect data from multiple HGCROCs and transmit them to the backend, using the lpGBT ASIC, through high speed (10Gbps), low power, radiation-hard links. The back-end DAQ functionality will be implemented in the Serenity ATCA hardware hosting two FPGAs. Each FPGA will receive ECOND data through 60 lpGBT links, align and store them to buffers. The buffers provide a means to smooth out the data flow sufficiently, to ensure that all downstream parts of the event data chain are able to handle the worst-case data rates. In addition, a L1T throttle signal can be asserted to reduce the probability of buffers overflowing. Since each ECOND can occupy the bandwidth of up to 2 lpGBT links, while multiple ECONDs can fit in one lpGBT, the DAQ firmware was designed in 30 highly configurable parallel processing units. Each unit processes data from two lpGBTs, capable of handling all possible ECOND/lpGBT combinations. Furthermore, data from the 30 Event Buffers are collected and sent to the central DAQ through 12 Links (SLinks) running at 16 Gbps. For each SLink, an engine block gathers the data from the selected Event Buffers and builds the SLink event. Depending on the number of event buffers per SLink (multiplexing ratio), each event buffer can be accessed by more than one SLink through an interconnecting logic. The selection can be different for each board, taking into account different input rates. The configuration data for the on-detector electronics is stored in control buffers in the DAQ FPGA. A control block associated with each buffer propagates the configuration data to the front-end electronics through the lpGBT control link offering both point-to-point and broadcasting transmission. A number of controller instantiations will be selected to optimise the tradeoff between resource utilization and configuration time. Finally the backend DAQ system receives the clock from the DTH and forwards it through the lpGBT control links to the on-detector electronics where it is recovered for use in the front-end. It also passes on the relevant fast control commands.

Primary author: MALLIOS, Stavros (CERN)

Co-authors: VICHOUDIS, Paschalis (CERN); DAUNCEY, Paul Dominic (Imperial College Sci., Tech. & Med. (GB)); DAVID, André (CERN)

Presenter: MALLIOS, Stavros (CERN)

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