Supporting document

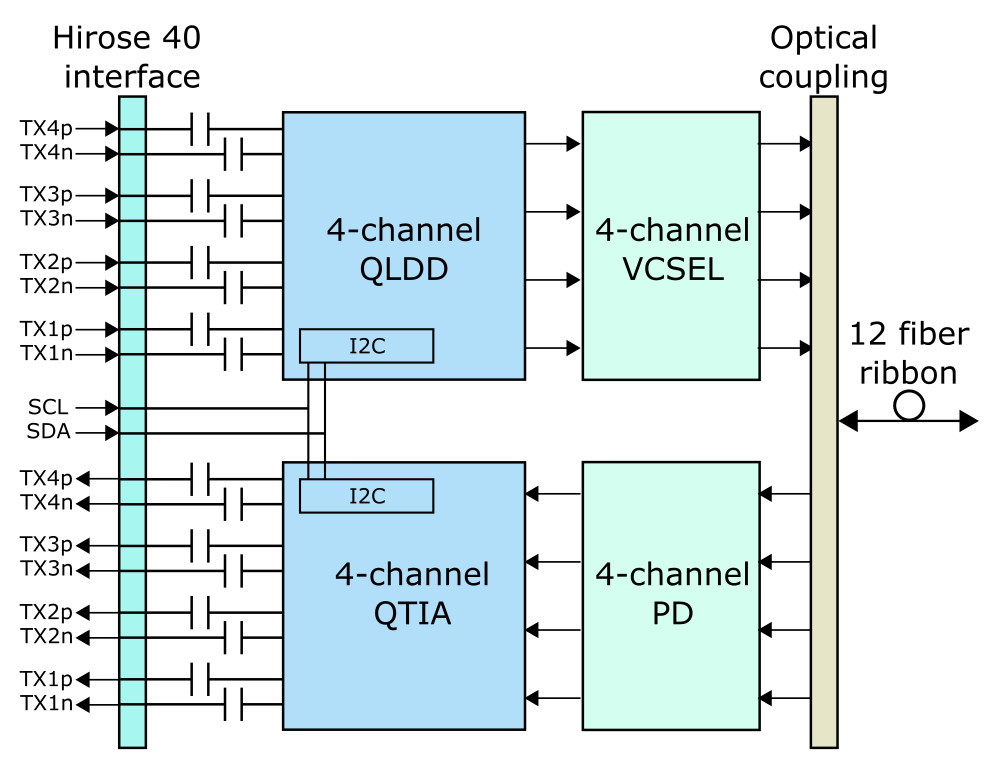


Figure 1. Block diagram of QTRx. The high-speed differential electrical signals are AC coupled. The electrical interface is a 40-pin Hirose connector with a 4 mm stacking height. The VCSEL and PD arrays are directly wire-bonded to QLDD and QTIA, respectively. The optical signal is coupled by an MT connector.

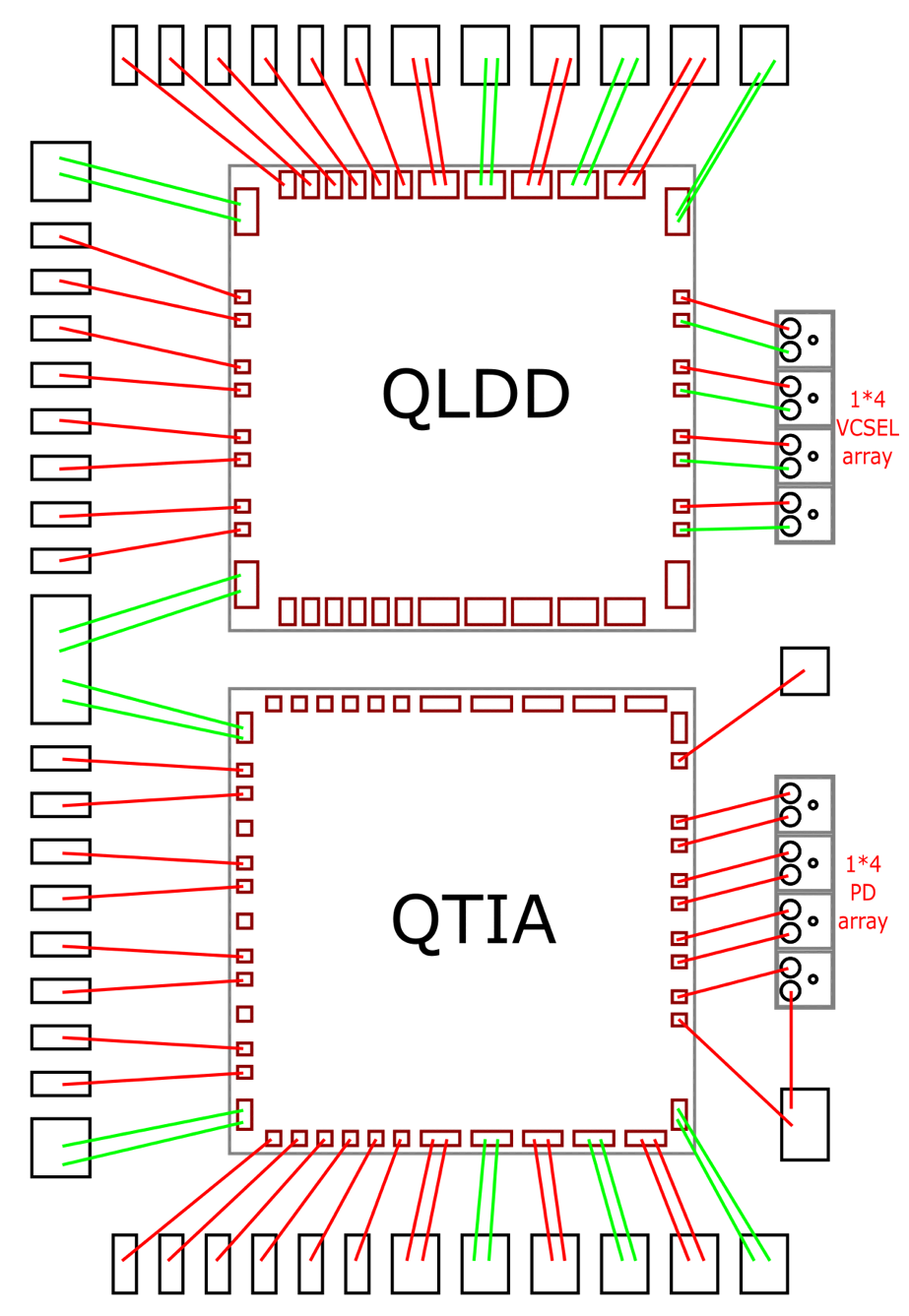
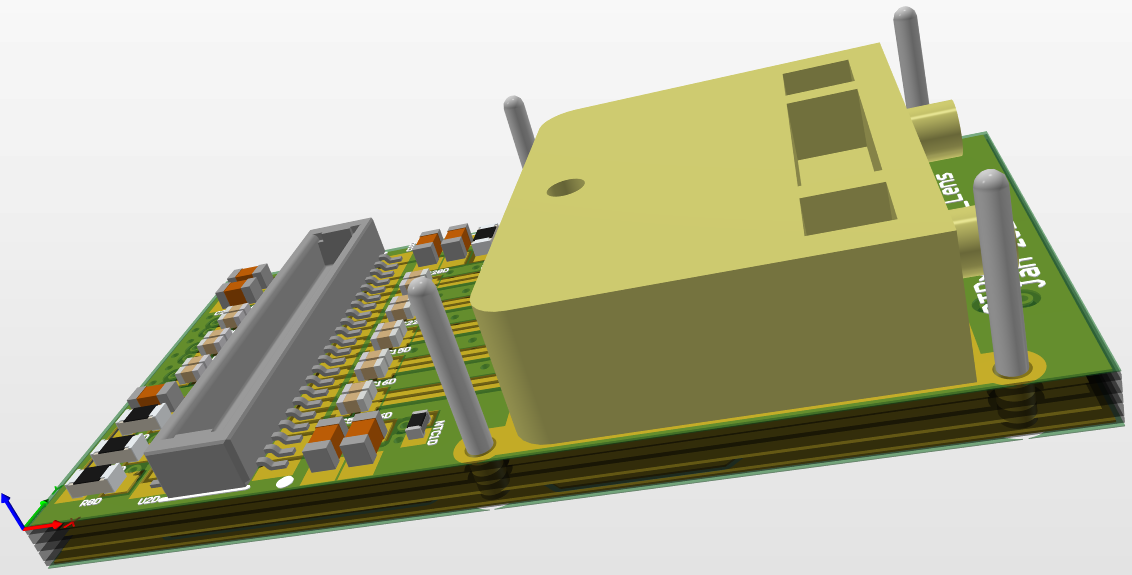
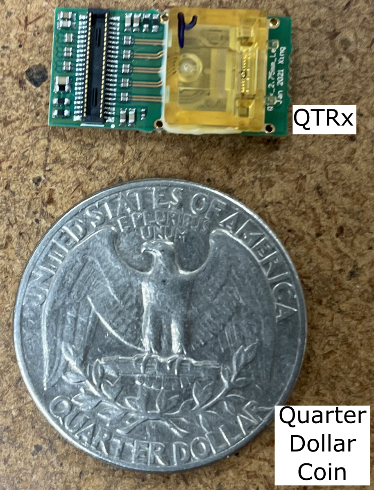


Figure 2. Bonding diagram of QTRx. The side pads of QLDD and QTIA are symmetrical, enabling an 8-Tx or 8-Rx configuration. One side wire bonding provides the control signals and the sufficient current. QLDD and QTIA share the same I2C bus with differing I2C addresses.

(a) (b)

Figure 3. 3D view of QTRx (a) and photograph of a QTRx compared with a US quarter dollar coin (b). All components are located on one side of the module PCB. QLDD, QTIA, VCSEL array and PIN array are covered by the lens. Four ground pins around the lens are used to anchor QTRx on the motherboard. The profile of the QTRx module is 20 mm (L) × 10 mm (W) × 5 mm (H).

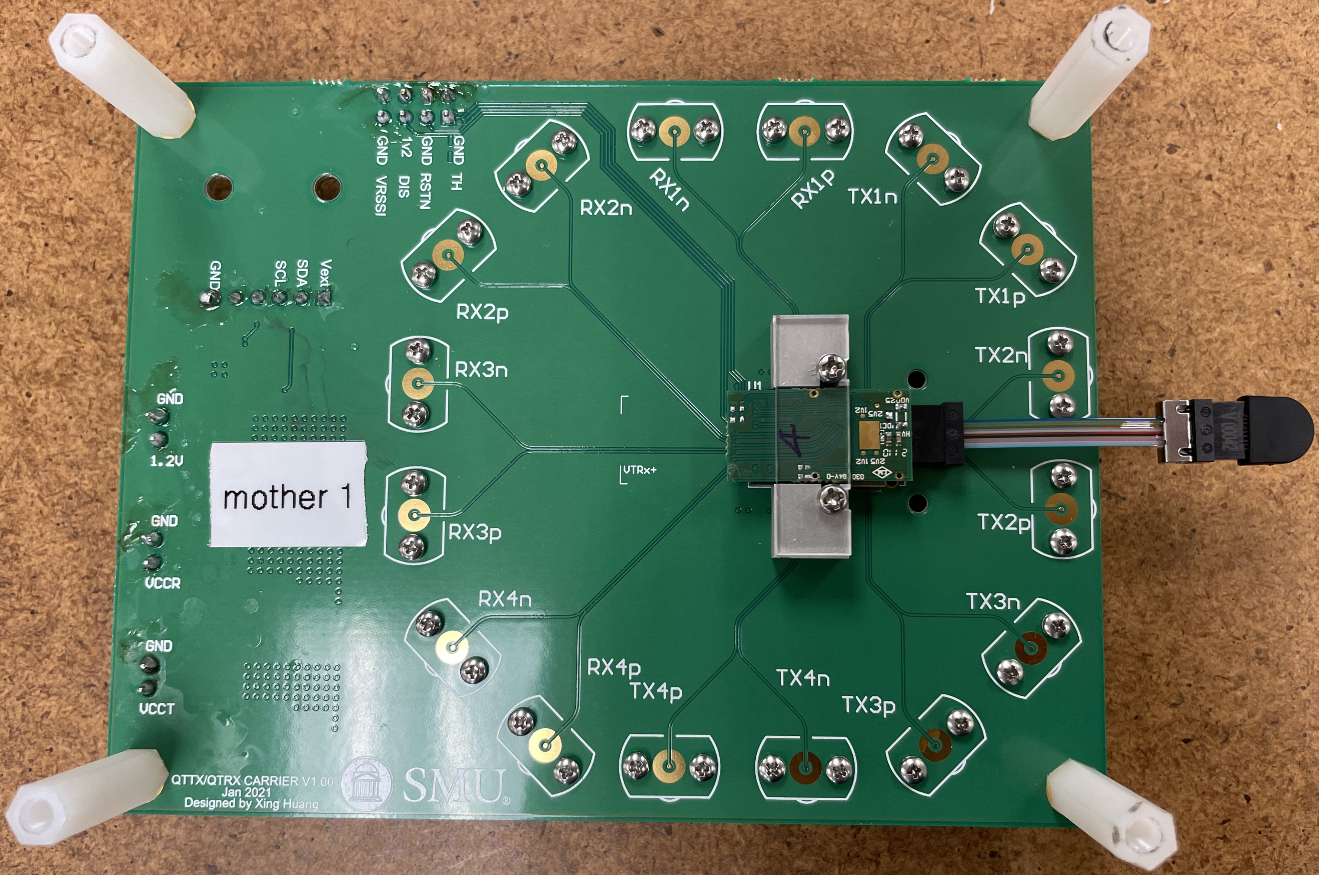


Figure 4. Photograph of a QTRx mounted on the motherboard.

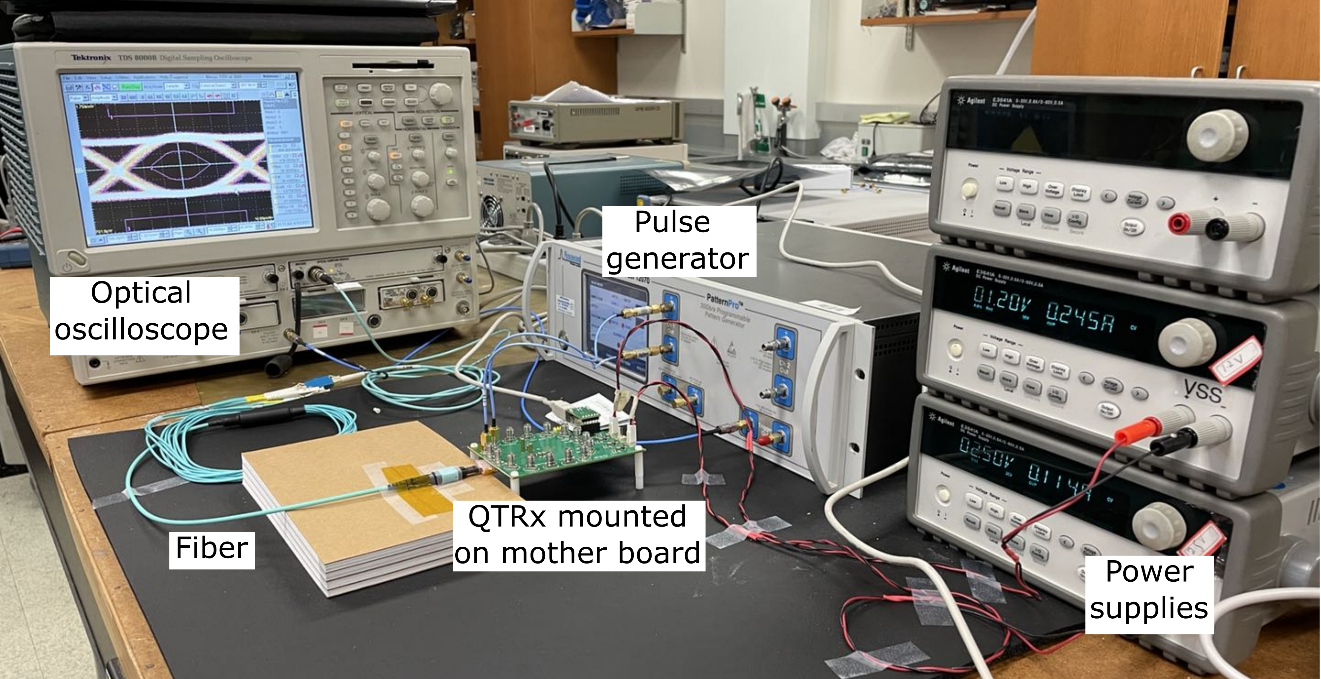


Figure 5. Photograph of the QTRx test setup.

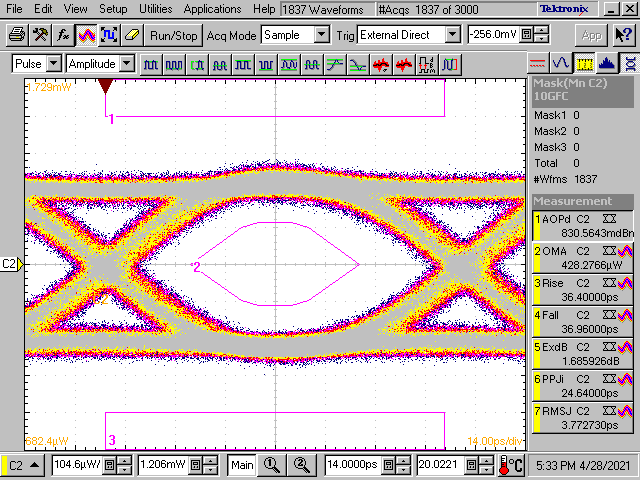


Figure 6. Eye diagram of a QTRx transmitter channel at 10 Gbps.

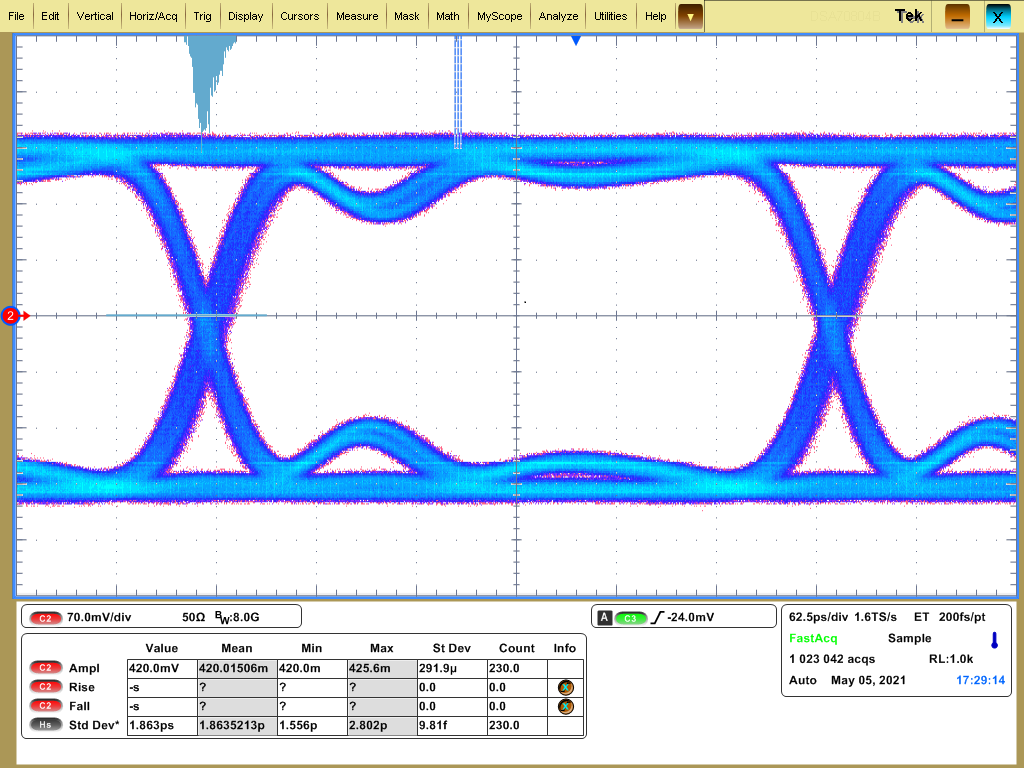


Figure 7. Eye diagram of a QTRx receiver channel at 2.56 Gbps

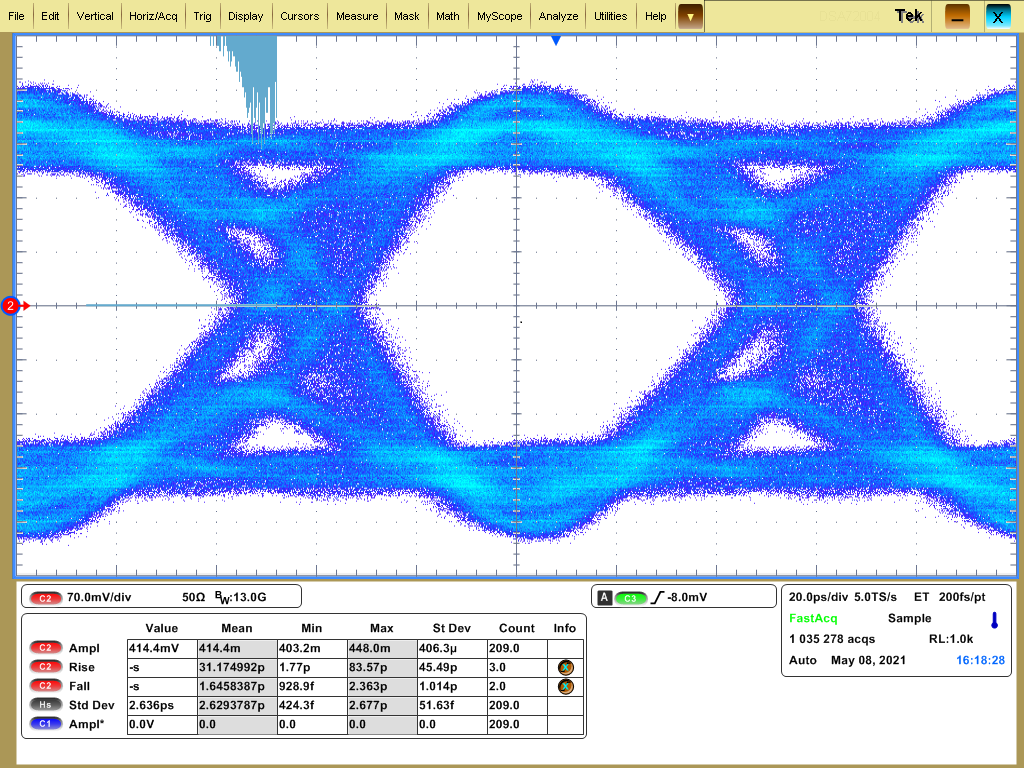


Figure 8. Eye diagram of a QTRx receiver channel at 10 Gbps