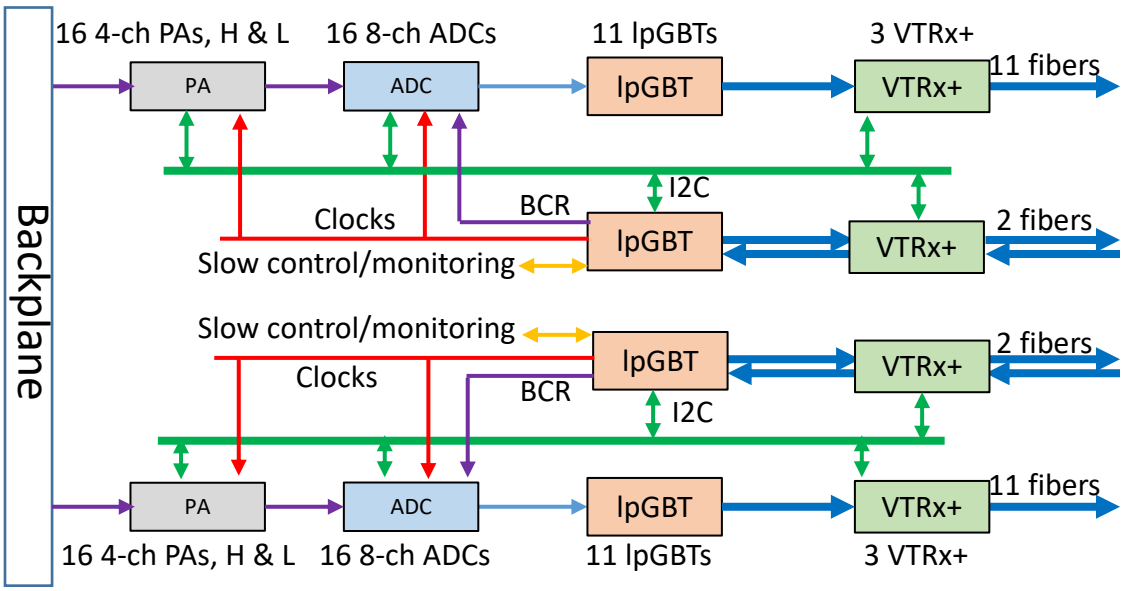

Figure 1. Block diagram of the FEB. In the figure, 128 analog channels are amplified and shaped in 32 4-channel Pre-Amplifiers (PAs, including shaping amplifiers) and then are digitized in 32 8-channel Analog-to-Digital Converters (ADCs). Each analog channel is digitized with two different gains (high and low shown in the figure) simultaneously in order to achieve a 16-bit dynamic range with a 12-bit ADC. The digitized data are transmitted from the detector to the off-detector counting room through optical links. These uplinks are called data links. We also need control links to provide clock and control/monitoring support. Each FEB has 22 simplex data links and 2 duplex control links. Optical links are based on lpGBTs [6] and VTRx+ modules. The lpGBTs responsible for data links will be called data lpGBTs, and the lpGBTs responsible for control links will be called control lpGBTs.

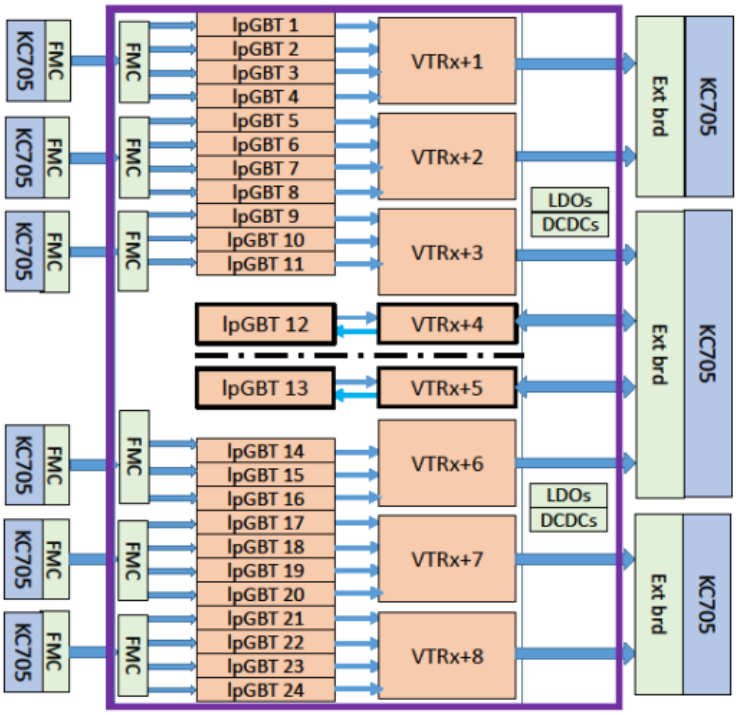

Figure 2. Block diagram of the prototype-link board. The board prototypes the full optical links of the future front-end board. The prototype-link board consists of 24 lpGBT chips and 8 VTRx+ modules. Two lpGBT chips, two VTRx+ modules, and two pairs of duplex fibers constitute the control links to distribute clocks and Bunch Crossing Reset (BCR) signals and control the whole FEB. These lpGBT chips and the VTRx+ modules operate in the transceiver mode. The rest 22 lpGBT chips operating in the transmitter mode, 6 VTRx+ modules with only transmitter channels in operation, and 22 simplex optical fibers form data links. The data links transmit detector data, which are emulated in FPGAs and injected through 6 FMC connectors, to the off-detector electronics.

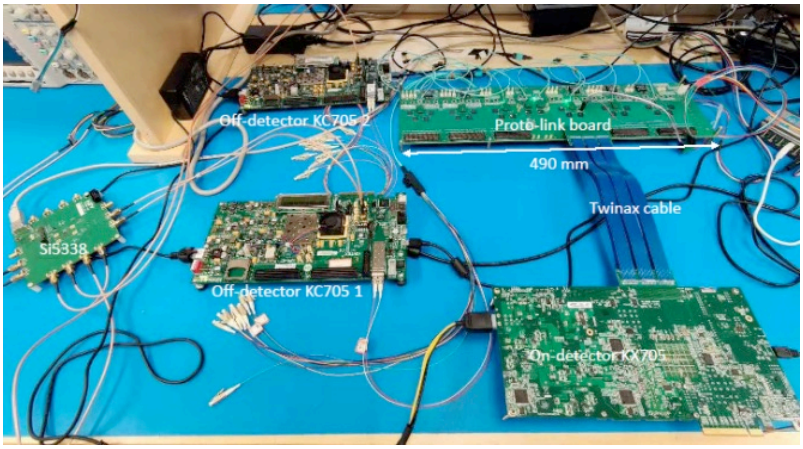

Figure 3. Photograph of the Porotype-link board and test setup. The Prototype-link board size is 490 mm x 134 mm and has 12 layers with the top and bottom layers in Panasonic Megtron6 high-speed materials. A Si5338 Evaluation board provides the clock for the whole test setup. Three FPGA evaluation boards (Xilinx KC705) are used to emulate the detector data and for the off-detector electronics.

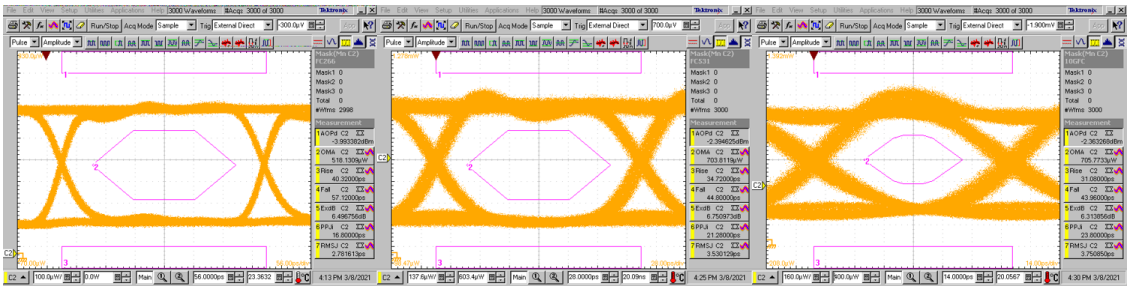

Figure 4. Eye diagrams of a downward control link at 2.56 Gbps (left), the upward control link at 5.12 Gbps (middle), and an upward data link at 10.24 Gbps (right).

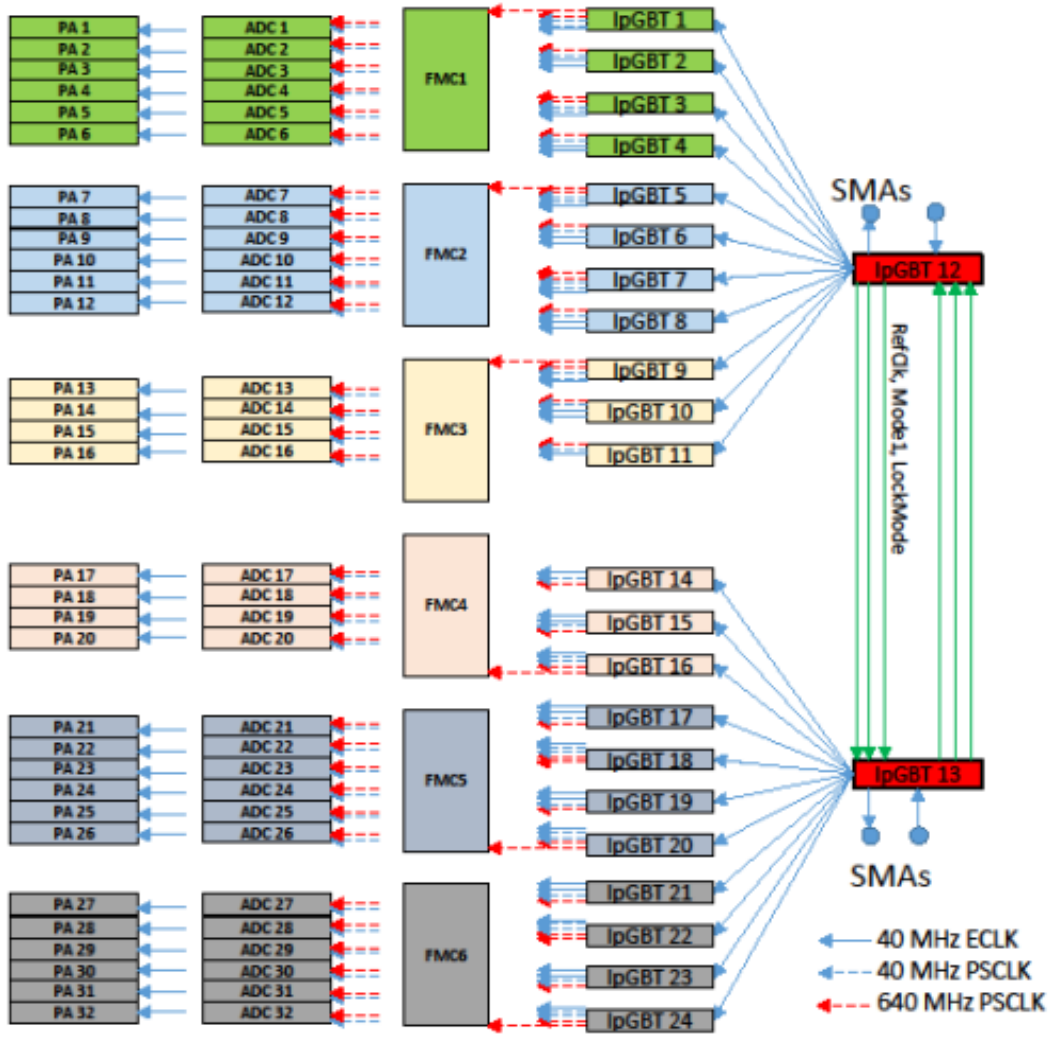

Figure 5. Redundant design of the clock distribution. Each control lpGBT (12 and 13) provides 40-MHz clocks to the data lpGBTs and the data lpGBT chips generate clocks for PAs and ADCs on the same half FEB board. LpGBT 12 on Half A supplies a clock (the pins ECLKOUT P/N) to the lpGBT 13 on Half B (pins RefClk P/N) and vice versa. LpGBT 12 controls the configuration pins of lpGBT 13 via digital I/O pins and vice versa.

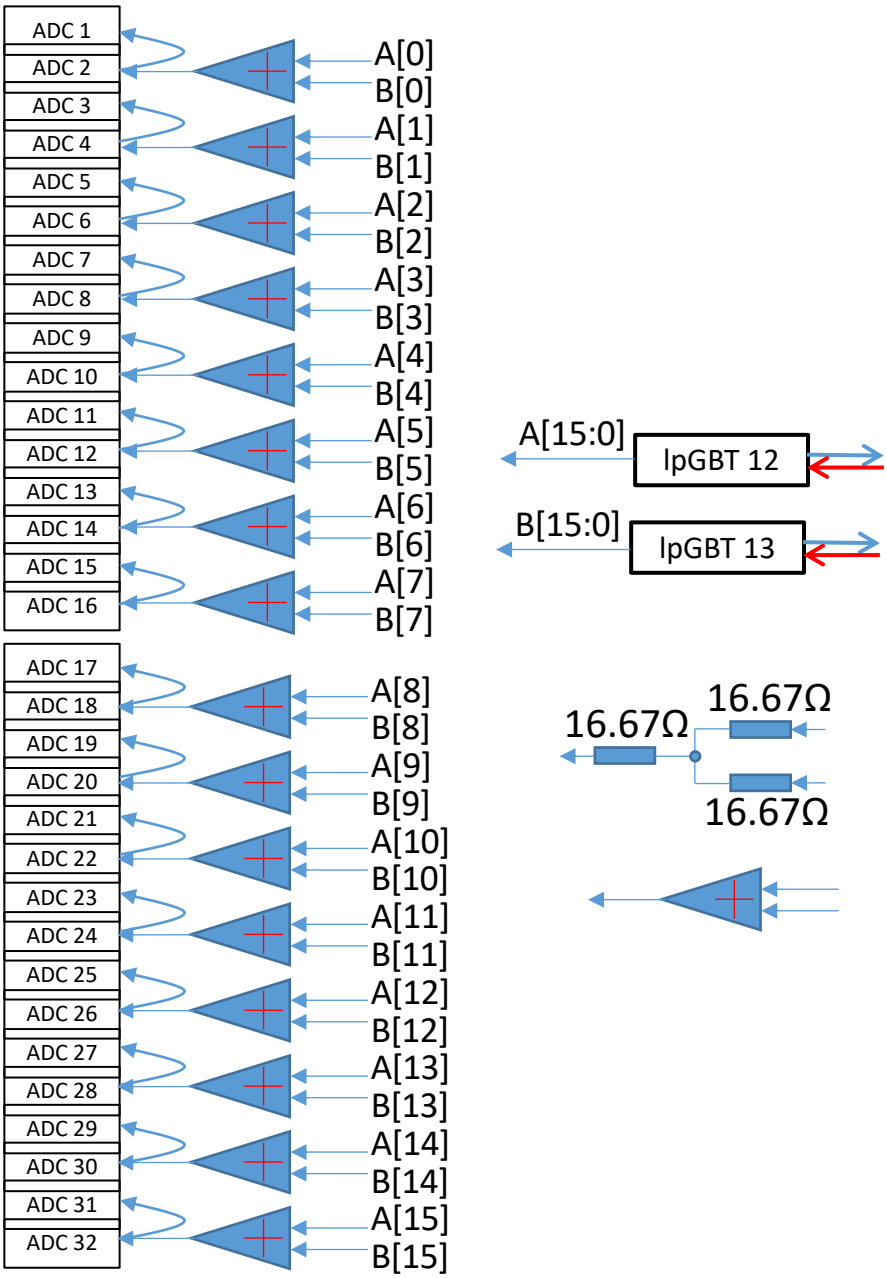

Figure 6. Redundant design of the BCR distribution. Each control lpGBT provides 16 BCR signals via electrical link output ports to 16 combiners. Each combiner is implemented in a Y-shape resistor network. The output of each combiner goes to an ADC and then daisy chains to another ADC. In the normal operation, the output ports of lpGBT 12 provide BCRs, while the EDOUT outputs of lpGBT 13 are set to be stable low. The driving strength of lpGBT 12 is set to be the maximum. If the downward control link of lpGBT 12 is lost (lpGBT 12 is still working), swap the settings of lpGBT 12 and lpGBT 13.

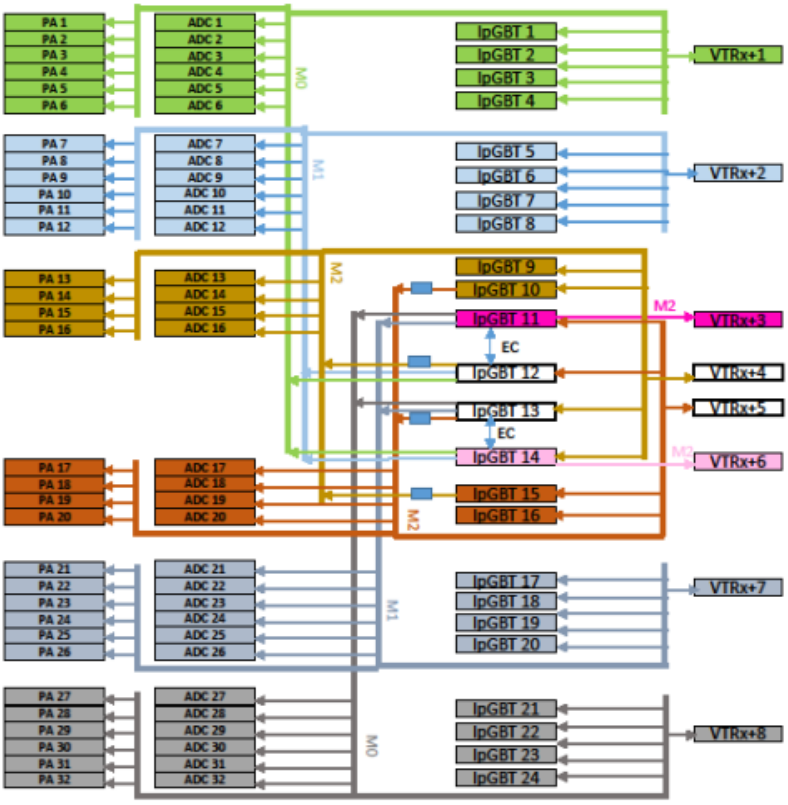

Figure 7. Redundant design of the I2C configuration. LpGBTs 12 and 13 are configured through the Internal Control (IC) channels and lpGBTs 11 and 14 via the External Control (EC) channel. Each I2C bus has dual controllers. In case of one control link is broken, lpGBTs 10, 11, 14, and 15 are used as I2C repeaters (For lpGBTs 10 and 15, only controller M2 is used). When lpGBT 12, VTRx+ 4, or the downlink fiber is broken, lpGBT 13 M0/M1/M2/EC and lpGBT 14 M2 operates normally. LpGBT 14 M0/M1 controls PA 1-12, ADCs 1-12, lpGBTs 1-8, and VTRx+ 1-2. LpGBT 13 M2 controls lpGBT 11 and indirectly VTRx+3. LpGBT 13 M2 through lpGBT 15 M2 controls indirectly PAs 13-16, ADCs 13-16, lpGBTs 9-10. As far as lpGBT 12 releases its buses, it is safe. If lpGBT 12 interrupts its buses, we lose half FEB2.

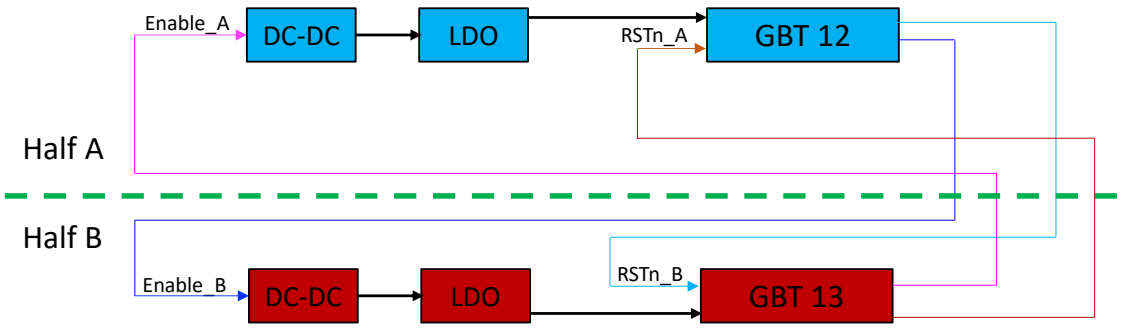

Figure 8. Crossover reset and power cycle design. All ASICs on the FEB can be reset or power cycled. Especially, lpGBT 12 can reset or power cycle lpGBT 13 and vice versa. The crossover reset and power cycle design has been verified on the prototype-link board.