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Development of a high bandwidth readout chain for the CMS Phase-2 pixel upgrade

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The CMS collaboration is building a new inner tracking pixel detector for the High-Luminosity LHC. Each pixel chip will be controlled with a single serial input stream at 160 Mbps and will send out data via four CML 1.28 Gbps outputs. The modules will be connected with up to 1.6 m long low-mass electrical links to the low power gigabit transceivers (lpGBT) and versatile transceivers (VTRx+) that send the data optically to off-detector electronics at 10 Gbps. The development and the characterization of these components will be presented along with system tests of the readout chain.

Summary (500 words)

The High-Luminosity LHC (HL-LHC) will provide CMS with a peak instantaneous luminosity of 7.5 × 10ˆ(34) cmˆ(−2) sˆ(−1) starting in 2027. Compared to the LHC, the HL-LHC will have up to 200 proton-proton collisions (pileup) per event and will shower CMS with a higher radiation fluence. To prepare for this data taking environment, the CMS Tracker will be fully replaced in the Phase-2 upgrade. The new inner tracker (the pixel detector) will have about two billion silicon pixels installed.

The detector will be built using hybrid pixel modules, and the sensor data will be processed by a custom readout chip (ROC) developed by the RD53 collaboration. The data from these pixel modules will be sent over up to 1.6 m long low-mass electronic links at 1.28 Gbps to port-cards mounted on the support structure inside the detector. The port-cards are dedicated printed circuit boards carrying the low power gigabit transceivers (lpGBT) and versatile transceivers (VTRx+) that concentrate the 1.28 Gbps electrical signals, convert them to 10 Gbps optical signals, and send them to back-end electronics that are based on FPGA boards.

The prototype low-mass electrical links are being developed and characterized with a series of measurements. The signal quality is assessed using eye diagrams to quantify the amplitude and jitter as well as identifying any distortion. Cross talk effects over electrical links bundled closely together are also studied. As a next step, single ROC cards and pixel modules are read out by electrical links connected to an FPGA board and/or a scope. These tests are used to understand the transmission characteristics of the ROC and the flex circuit on the module and how to optimize the transmission parameters of the CML drivers (amplitude, pre-emphasis) of the chip. Eye diagrams and bit error rate tests are used to quantify the signal integrity and identify any source of distortion in the electrical part of the readout chain. In parallel, dedicated setups with the port-cards reading out single ROC cards with short coaxial cables have been used to test the prototype port-card and validate the optical part of the readout chain. Finally, the entire readout chain is put together in an ultimate readout system test where pixel modules are read out by long electrical links connected to port-cards, which send the optical signals to the back-end FPGA boards. The developments and test results described above will be presented in this contribution.

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