The Versatile Link + Demo Board (VLDB+)

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TWEPP-21

EP-ESE ELECTRONIC SYSTEMS FOR EXPERIMENTS

Abstract

The Versatile Link Plus Demonstrator Board (VLDB+) is a board designed by CERN's EP–ESE group to provide an evaluation kit for the new Versatile Link ecosystem (VL+). This reference design gathers four custom and radiation hard devices, namely, the Low–Power Gigabit Transceiver (lpGBT), the Versatile Link Plus Transceiver (VTRx+) and the two DC–DC converters (bPOL or FEASTMP). These components are common to some of the HL–HLC experiments and constitute the main elements of the board. The VLDB+ is already being extensively used by several experiments to get acquainted with the whole ecosystem in order to facilitate their final Front–end system design.

Control

The lpGBT on the VLDB+ has to be externally controlled either through IC using the optical fiber or through I2C channel using a ribbon cable. For this latter, we provide a Raspberry Pi 4B (completed with a Translator Board) which runs the so–called PiGBT software. The Raspberry Pi (RPi) can be controlled either by WiFi or by physical Ethernet connexion.

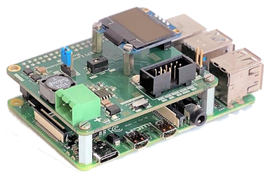

Figure 2: Raspberry PI Toolkit made of RPi 4B and custom Translator Board

Once the user is connected, he can open the PiGBT Graphical Web Interface using the computer's browser and many of the lpGBT features will be displayed in an orderly fashion as shown in Figure 4. The user can easily configure and read back each register and the lpGBT will automatically be programmed after each modification. The ribbon cable interconnecting VLDB+ and RPi Control Toolkit (on the bottom of Figure 3) uses the I2C bus to configure the ASIC, but features also additional pins to control the lpGBT Mode and Reset as well as the DC–DC's Enable inputs. In this manner, the user is also capable to remotely change the transmission mode, reset the chip and power cycle the whole board. It is worth noting that the PiGBT Graphical Web Interface is also available online as a demonstrator, allowing users to prepare the lpGBT without being physically connected to the chip.

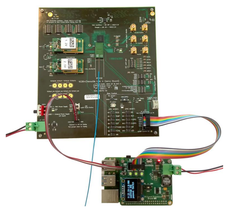

Figure 3: RPi Toolkit interfacing with the VLDB+

Finally, the RPi control toolkit offers the possibility to fuse the lpGBT housed on the VLDB+ via a 2–pin specific connector (left of Figure 3). Therefore, the user can fine–tune the most optimal lpGBT configuration using the PiGBT Graphical Interface, save it and fuse it on the ASIC when ready, thanks to the automatized procedure implemented in the toolkit.

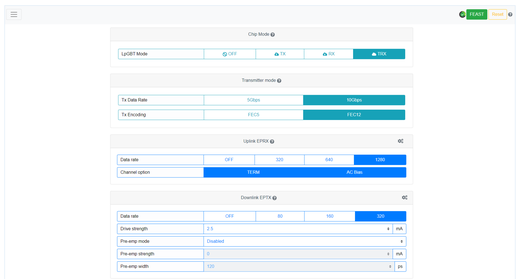

Figure 4: PiGBT Graphical Web Interface

Overview

VTRx+: VL+ Optical Transceiver with four transmitters and one receiver. It is used for the lpGBT data transmission and reception through the optical fiber. The VLDB+ can also work with a commercial SFP+. The image shows the bottom of the VTRx+, featuring the low profile connector and the optical block.

DC–DC converters: FEASTMPs supplying 1.2V to the lpGBT and VTRx+, 2.5V to the VTRx+ and 3.3V when using an SFP+ as transceiver. The use of the bPOL ASICs on the VLDB+ are also foreseen on a specific mezzanine.

Tstout: The lpGBT TSTOUT configurable signals are present in the VLDB+ for debugging purposes. These signals can be analysed by either probing in the middle of the pad or using two Samtec's CCH–J–04 connectors together with the RF25S SMA cables for a better analysis.

Power: The VLDB+ features a tri–state switch to select the source of the 12V to be provided at the DC–DC's inputs: either via the Evaluation Kit FPGA connected as FMC carrier board (FMC mode) or from an external voltage supply (Standalone mode).

Fusing: The lpGBT housed on the VLDB+ can be fused through a 2–pin connector where external 2.5V are required during the fusing process.

FMC: Two FMC–HPC connectors are located on the bottom of the board so that it can be plugged as a double–width mezzanine card into an FPGA Evaluation Kit. These connectors interface all the lpGBT eLink data and clocks as well as the I2C Masters, Analog peripherals, GPIOs and Resetout signal. Four protection switches and a warning LED are present to protect the lpGBT against an overvoltage. A small EEPROM is also present to comply with the VITA standard.

(Pictures not to scale)

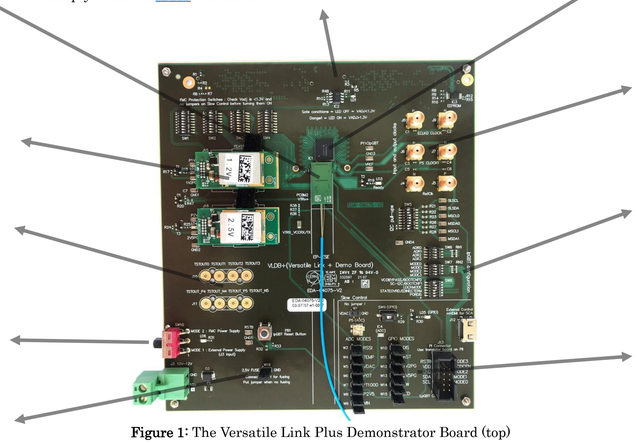

Figure 1: The Versatile Link Plus Demonstrator Board (top)

lpGBT: Low Power Gigabit Transceiver ASIC dedicated to serialization, deserialization, forward error correction and clock recovery.

SMA connectors: The VLDB+ features six SMA connectors, from top to bottom: The first SMA pair (J8 and J9) corresponds to the lpGBT's eLink output clock 0. The second SMA pair (J6 and J7) corresponds to the lpGBT's Phase Shifter output clock 1. The last pair (J4 and J5) corresponds to the lpGBT's Reference input clock.

Configuration switches: The configuration switches are necessary in the VLDB+ to manually select the lpGBT address, mode and configuration pins (some of them can also be remotely configured). These switches also allow to add and remove pull–ups from the I2C Masters 0 and 1 as well as for the lpGBT I2C Slave bus to fit specific user's configurations.

Slow Control: In the slow control area we have:
1) several lpGBT ADC/DAC and GPIO pins that can be connected to different features (VTRx+ RSSI, FEASTMP1V2 PG, …) through jumpers,
2) the mini HDMI connector used for the communication between lpGBT and GBT–SCA communication and
3) The Raspberry Pi connector for the remote control of the lpGBT and the board housekeeping.

Features

VERSATILE LINK EMULATION

One of the main goals of using the VLDB+ is to have the possibility to test the lpGBT characteristics without requiring a complete Front–End system. One of the most common use cases is to create a full downstream and upstream link, from Back–End to Front–End. By using the dual FMC interface, we connect the board to a compatible FPGA Evaluation Kit. The FPGA can interface with the VLDB+ playing both roles, as a Back–End via the VTRx+ and the optical link in one side and as a Front–End ASIC via the dual FMC system on the other side. This system is shown in Figure 5a.

SLOW CONTROL

Another useful feature that offers the VLDB+ is the use of the EC channel to communicate with the GBT–SCA (Slow Control ASIC). Employing a mHDMI cable we are able to interconnect the VLDB+ and the former VLDB, featuring a GBT–SCA, through the mHDMI connectors located on both boards, thereby creating an interface between lpGBT and GBT–SCA through EC. This system is shown in Figure 5b.

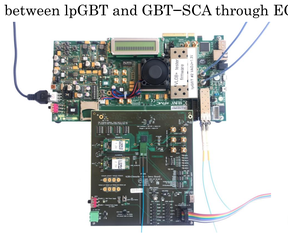

Figure 5a: Interface between VLDB+ and VC707 Evaluation Kit FPGA

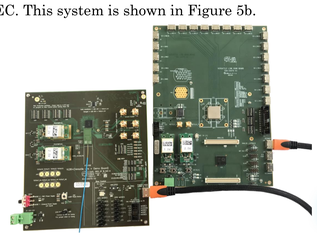

Figure 5b: Interface between lpGBT and GBT–SCA using the VLDB and VLDB+

Some simple features available in the lpGBT are the Analog and GPIO interfaces. In the VLDB+ these features are on the Slow Control area. By putting a jumper we can interconnect, for instance, the ADC1 with the VTRx+ internal thermistor. In total seven ADCs and six GPIOs that can be connected to different devices. In addition, the DAC can be either connected to the ADC2 or probed through a 2–pin connector.

FUSING

Another common lpGBT feature which is not easily testable on a Front–End card is the Fusing. The fusing process on a VLDB+ can be easily done using the RPi Control Toolkit. Once the lpGBT is fused, the user can thoroughly test its automatic initialization and the new window of possibilities that this offers.

Performance

The Figure 6 shows the eye diagram of the optical lpGBT uplink at 10.24Gbps in transceiver mode using a VC707 as back–end. The data were generated from the FPGA "Front–End side" as in the setup of the Figure 5a. The high–speed traces, properly controlled in terms of impedance, together with the good performance of the VTRx+ transceiver offer a clean uplink eye diagram.

The data transmission and reception is one of the most critical aspects in the lpGBT. Thereby we ensured a good impedance control of the data and clock signals, from the 2.56/10.24Gbps high–speed lines to the eLink receivers, transmitters, and eLink clocks.

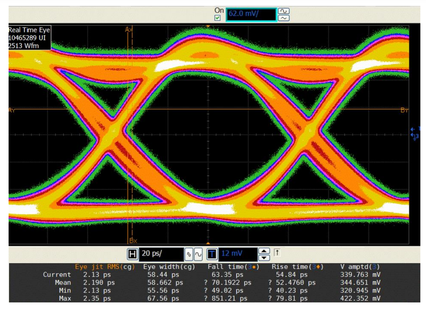

Figure 6: Eye diagram of the VLDB+ Uplink at 10.24Gbps

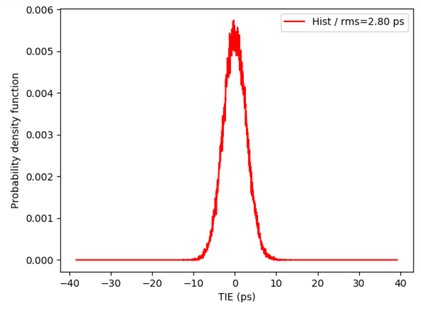

Figure 7: Time Interval Error of the ECLK0 signal (40MHz) made available via the VLDB+ SMA connectors

The VLDB+ layout was designed with care to limit all sources of noise. For example, to limit reflections, the six SMA on the VLDB+ were implemented with extra large antipads (area between signal and copper plane). Results show that this feature reduces reflections by 65% with respect to the classical footprint. Through the SMAs the user can, among other things:

- Use the clock output or the phase shifter clock as a reference for another lpGBT.
- Perform characterisation and timing analysis (jitter, phase noise, phase determinism,…). The Figure 7 shows a TIE analysis done in the VLDB+ through the ECLK0 SMAs.
- Get used to the Phase Shifter Clock functionality by playing with the lpGBT configuration and monitoring the signal directly from the SMA.
- Ensure that the external clock signal you can provide to the lpGBT reference clock can make the chip lock.

Status

The VLDB+ (so far featuring an lpGBTv0 but a version compatible with lpGBTv1 is available) is already a useful board for many users from CERN and from external institutes who want an ecosystem to gain experience on the lpGBT and the VTRx+. We provide all the necessary tools to build a full Versatile Link+ prototype system between Front–End and Back–End electronics. Users can employ all possible options that this board offers to safely start designing their own board, test and improve their firmware and software or to validate and prepare lpGBT configurations.

Furthermore, not only users benefit from the availability of the VLDB+, but also the VL+ team. Thanks to the VLDB+, a final system can be emulated, giving the possibility at early stages of the project to detect problems, test all the VL+ and power devices together on the same setup and be as close as possible to the users' systems in order to support them efficiently. Finally, the radiation hard nature of the board allows performing radiation tests of the complete VL+ ecosystem.

References

Where can I know more about the VLDB+?
You can navigate our Website where you will find all the necessary info.

Where can I order a VLDB+ Kit?
Go to Order, sign–on and fill in the required fields.

Is there any VLDB+ manual?
Sure! The Manual is constantly being updated.

If I have a problem with the VLDB+, what can I do?
In case of doubt or issues we give constant support to our users through our Discourse forum and also by email.

Acknowledgements

Many thanks to the whole lpGBT designers team for their precious advices and constant support.