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The Versatile Link+ Demo Board (VLDB+)

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The Versatile Link Plus Demonstrator Board (VLDB+) is a board designed by CERN's EP-ESE group to provide an evaluation kit for the new Versatile Link ecosystem (VL+). This reference design gathers three custom and radiation hard devices, namely, the Low-Power Gigabit Transceiver (lpGBT), the Versatile Link Plus Transceiver (VTRx+) and the FEASTMP DCDCs. These components are common to some of the HL-HLC experiments and constitute the main elements of the board. The VLDB+ is already being extensively used by several experiments to get acquainted with the whole ecosystem in order to facilitate their final Front-end system design.

Summary (500 words)

The Versatile Link Plus Demonstrator Board (VLDB+) is a board designed by CERN's EP-ESE group to provide an evaluation kit for the new Versatile Link Plus ecosystem. This reference design includes only qualified radiation hard components, also designed at CERN, such as the Low-Power Gigabit Transceiver (lpGBT), the Versatile Link Plus Transceiver (VTRx+) and the FEASTMP DCDCs, common to some of the HL-HLC experiments, as ATLAS and CMS, and composing the main elements of the board.

In the VLDB+, the lpGBT and the VTRx+ work together to support the main interface of the board: the high-speed bidirectional data transmission link over the optical fiber. In addition, the lpGBT features ad hoc electrical interfaces called eLinks. These eLinks are provided through a second interface that are the two FPGA Mezzanine Card connectors (FMC), which share all the eLink inputs and outputs. Additionally, not only the eLinks are available on the FMC interface: the lpGBT's GPIOs, Analog Peripherals, I2C master and the Resetout signal are also present.

As the dual FMC interface housed in the VLDB+ complies with the VITA standard, the board can be connected as a mezzanine to a compatible FPGA Evaluation Kit, as the VC707. This FPGA-VLDB+ system provides an optimal way to work with the lpGBT-VTRx+ pair: the FPGA can interface with the VLDB+ as a back-end (via the VTRx+ and the optical link) and a front-end (via the FMC) system at the same time.

The VLDB+ can also be used as a standalone board. In this case, the connectivity is of course limited with respect to the mezzanine mode, but there is still access to some clock signals, test outputs as well as slow control features available on the board –enough to check ad-hoc lpGBT configurations or to try out some slow control functionalities.

Moreover, in the VLDB+ the control of the lpGBT using the I2C interface is performed through a 10-pin connector, so that a custom external RaspberryPI Kit (RPI Kit), composed of a Raspberry Pi 4 and a Translator Board, can be connected to it. The RPI Kit operates with a web interface called PiGBT and offers a simple way to control the lpGBT configuration.

The VLDB+ board offers an excellent opportunity to be introduced to and get acquainted with the extremely versatile VL+ ecosystem. This presentation describes in depth a wide range of board features that will enable the users to obtain the best hardware configuration for their initial needs.

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