

# Frontend and backend electronics for the ATLAS New Small Wheel Upgrade

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The present ATLAS innermost endcap muon station will be replaced by a New Small Wheel (NSW) detector to handle large trigger and readout data rates expected at high luminosity LHC runs. Two new detector technologies, Resistive Micromegas (MM) and small-strip Thin Gap Chambers (sTGC), will be used for triggering and tracking. A common readout path and two separate trigger paths are developed. It is challenging to integrate and commission this complicated detector-electronics system with 128 MM and 192 sTGC detector modules and 2.4M readout channels. I will discuss the design of the NSW electronics and the status of detector-electronics intergration.

## Summary (500 words)

To maximize the physics reach, the Large Hadron Collider (LHC) plans to increase its instantaneous luminosity to  $7.5 \times 10^{34}$  cm<sup>-2</sup>s<sup>-1</sup> and deliver 3,000-4,000 fb<sup>-1</sup> of data at a center-of-mass energy of 14 TeV. The luminosity increase will drastically impact the ATLAS detector, trigger and readout system. To retain the good precision tracking and trigger capabilities in the high background environment of the high-luminosity LHC, the present ATLAS innermost endcap muon detector will be replaced with a New Small Wheel (NSW) detector. The NSW will feature two new detector technologies, Resistive Micromegas (MM) and small strip Thin Gap Chambers (sTGC). Both detectors will be used for muon triggering and precision tracking.

A common readout path and two separate trigger paths are developed for these two detector technologies. The frontend electronics are implemented in about 8000 printed circuit boards including the design of four ATLAS customly-designed ASICs capable of driving trigger and tracking primitives to the backend trigger processor and readout system. The readout data flow is performed through a high-throughput network approach. Tasks such as time, trigger and control signal distribution and readout are performed by several ASICs developed by CERN.

The large number of readout channels, short time available to prepare and transmit trigger data, large volume of output data, harsh radiation environment, and the need of low power consumption all impose great challenges on the design, integration and commissioning. Extensive work is ongoing with the NSW detector and electronics at CERN. It is extremely challenging to perform integration and commissioning for this large and complicated detector-electronics system with 128 MM and 192 sTGC detector modules (each module contains four layers of MM or sTGC detector) and ~2.4 million readout channels. Various issues have been found and corrective actions have been implemented. The overall design of the NSW frontend and backend electronics and the status of the detector-electronics intergration and commissioning will be discussed, along with results from noise runs and cosmic rays.

**Primary authors:** ATLAS MUON COLLABORATION; SUN, Siyuan (University of Michigan (US))

**Presenter:** SUN, Siyuan (University of Michigan (US))

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