Design, Production, Burn-in and Tests of the hybrid circuits of the Upstream Tracker at the LHCb detector

Federico De Benedetti, INFN Sezione di Milano
On behalf of the LHCb UT group

Outline

Introduction

- LHCb and Upstream Tracker overview
- SALT chip overview

Hybrid Circuit Design

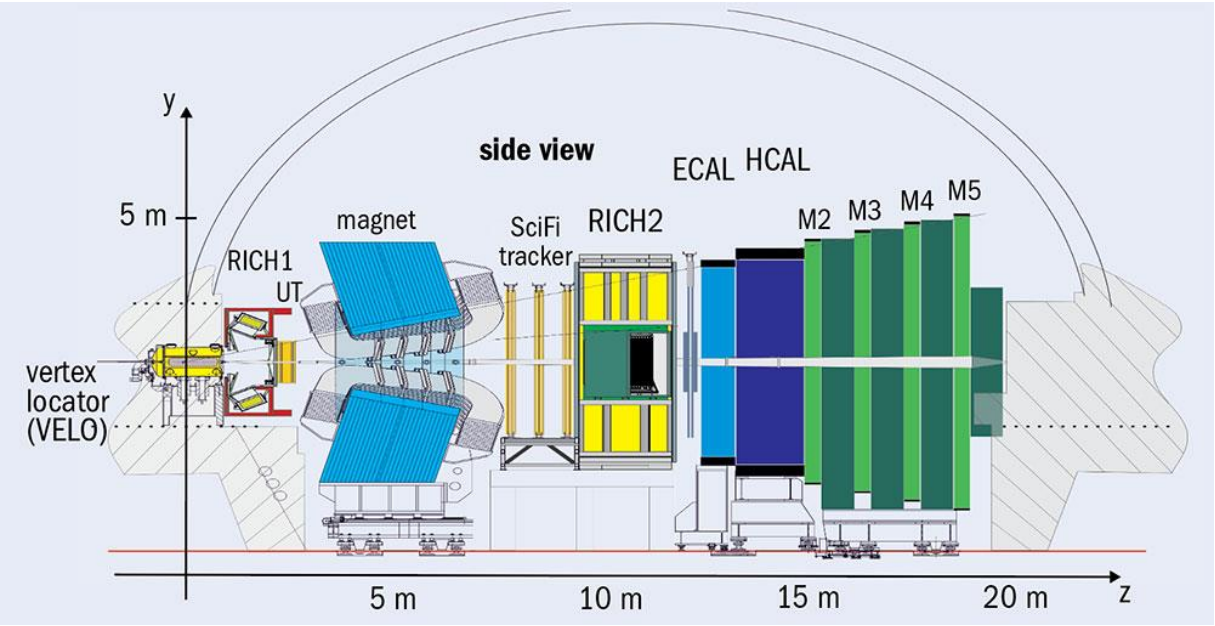
- Hybrid layout
- Hybrid simulations
- Hybrid prototype tests

Hybrid Circuit Production

- Panel design
- ASIC sorting, gluing and alignment
- Wire bonding
- Burn-in test, hardware and software
- Electrical tests and grading
- Visual inspection and shipment

Summary

LHCb Detector - Overview



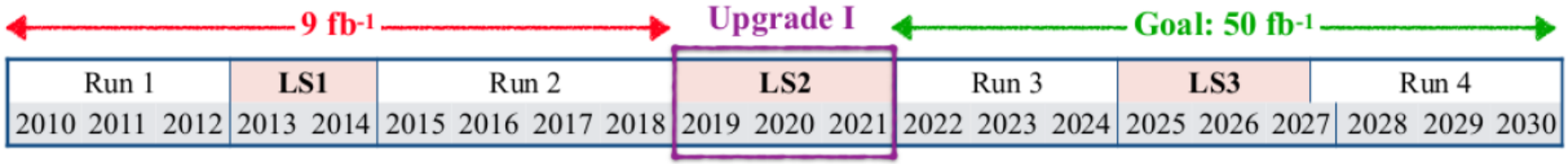
Single arm forward spectrometer

- Coverage: 2<η<5
- Designed for CP violation studies in b and c hadrons decays and their rare decays

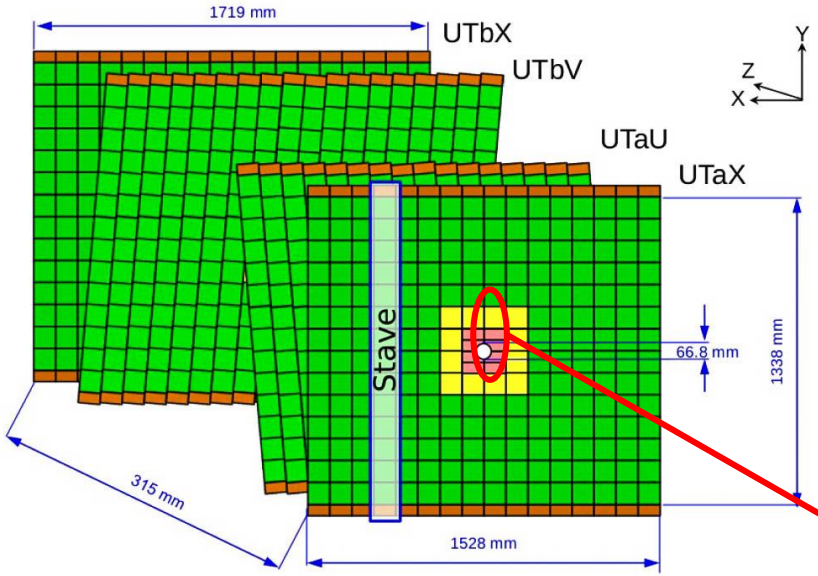
Precision of many physics measurements at LHCb statistically limited at the end of Run 2

LHCb Upgrade I - Run 3

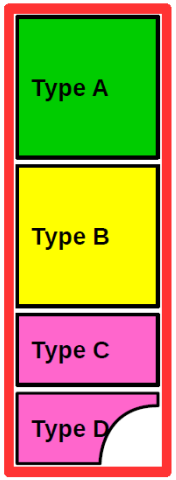
- 5x luminosity→ L= 2*10^33cm^-2s^-1
- Goal 50 fb^-1 by 2030
- 40 MHz readout and full software trigger
- New tracker (VELO, UT, SciFi)
- New optics and PMTs of RICH 1, RICH 2

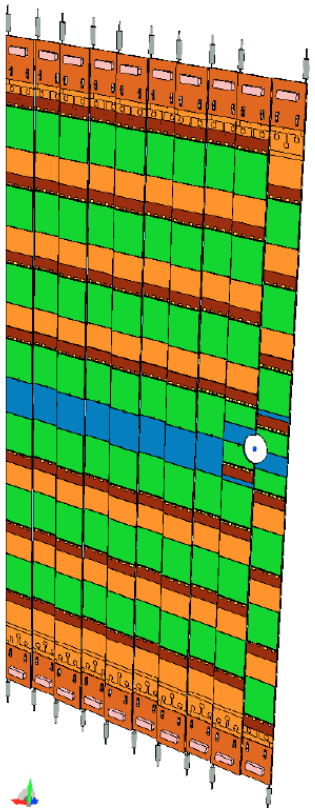


Upstream Tracker - Overview



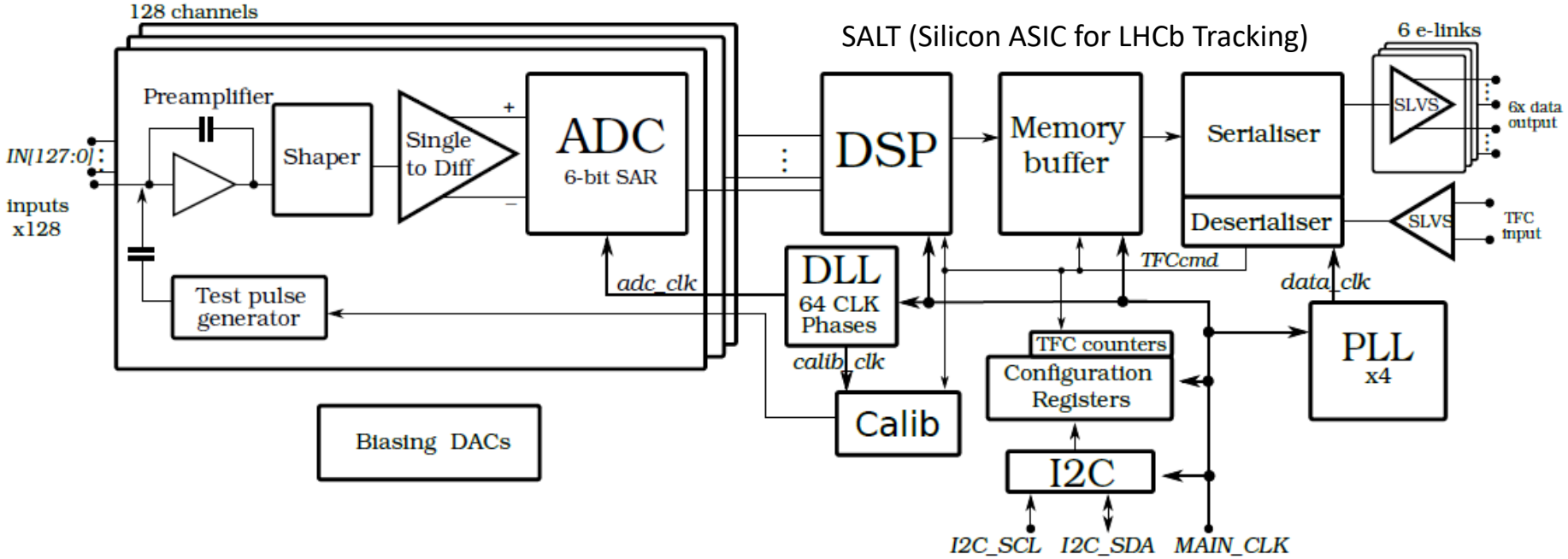
Sensor	Technology	Thickness	Length	Pitch	#
A	p-in-n	320 um	99.5 mm	**187.5 um**	888
B	n-in-p	250 um	99.5 mm	93.5 um	48
C	n-in-p	250 um	50.0 mm	93.5 um	16
D	n-in-p	250 um	50.0 mm	93.5 um	16

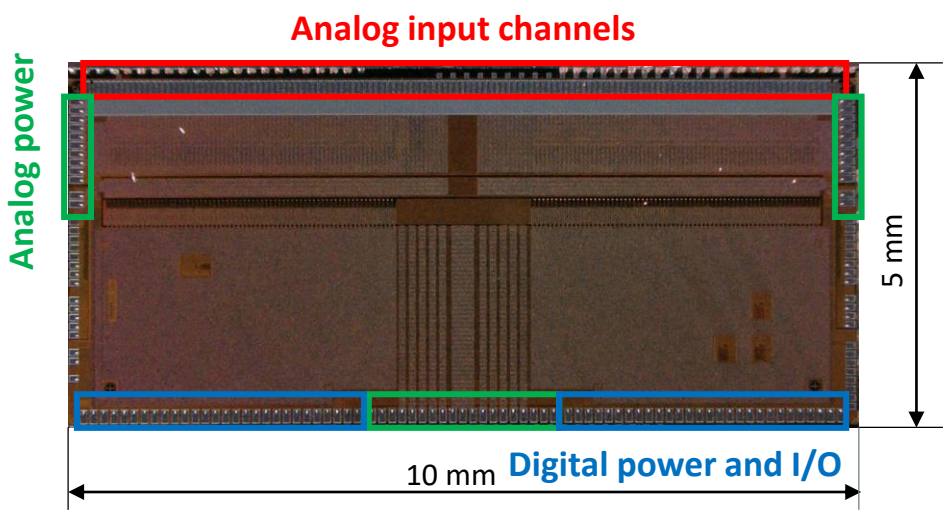




- Four detection layers constructed using vertical "**staves**".
- Single side silicon sensors mounted on both sides of the stave to eliminate any acceptance gap
- Finer segmentation in high-occupancy region.
- Inner-most sensors with circular cut-outs to maximize the acceptance near the beam line.
- Measure of XUVX coordinates: 0° and ±5° strips providing stereo information.
- Four single side silicon sensor designs to cope with occupancy and radiation, produced by Hamamatsu.
- Evaporative CO2 cooling system embedded into the stave

SALT ASIC Overview





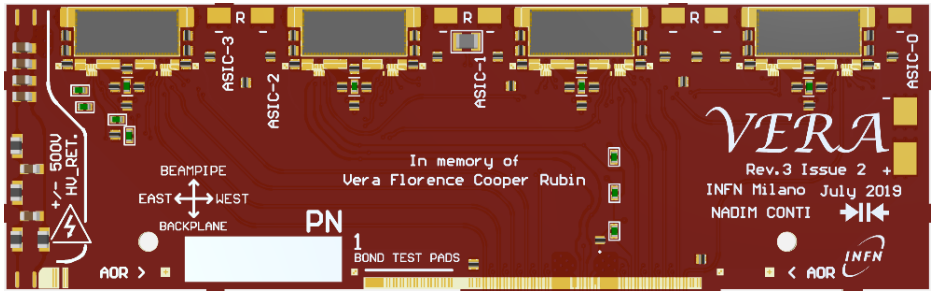
- 128 channels. One 6 bit @40MHz ADC for each channel
- Digital Signal Processing (DSP) with **built-in common mode suppression algorithm and zero suppression.**
- Digital blocks: PLL, DLL, TFC, I2C, serializer, SLVS I/O, biasing DACs…
- Approx 550 mW of power dissipation
- *Total number of ASICs: 4192*
- *Total number of channels: 536000*
- PSRR lowest point near 40 MHz, hybrid PDN must be designed accordingly
- **Latest version: SALT V3.9 (improved SEU)**

Hybrid Circuit Design and Test

- Hybrid layout
- Hybrid simulations
- Hybrid prototype tests

Hybrid Circuit Design

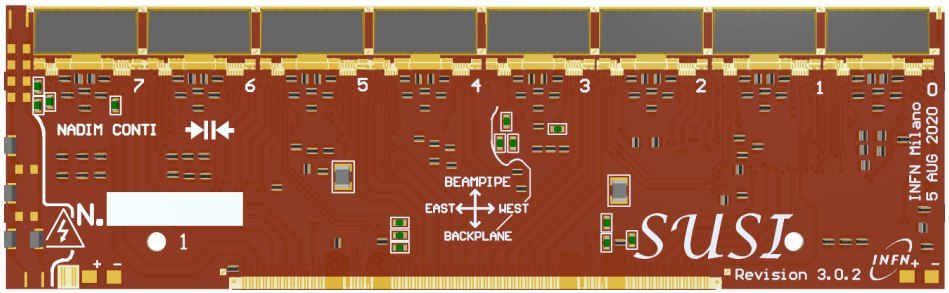
VERA Hybrid



- 4 ASICs
- Sensor: Type A
- 4 copper layers, thickness: 320um
- 12 E-Links
- N. of produced hybrids 1080

https://edms.cern.ch/document/2631774/1

SUSI Hybrid



- 8 ASICs
- Sensor: Type B,C,D
- 4 copper layers, thickness: 440 um
- 40 E-links
- N. of produce hybrids 110

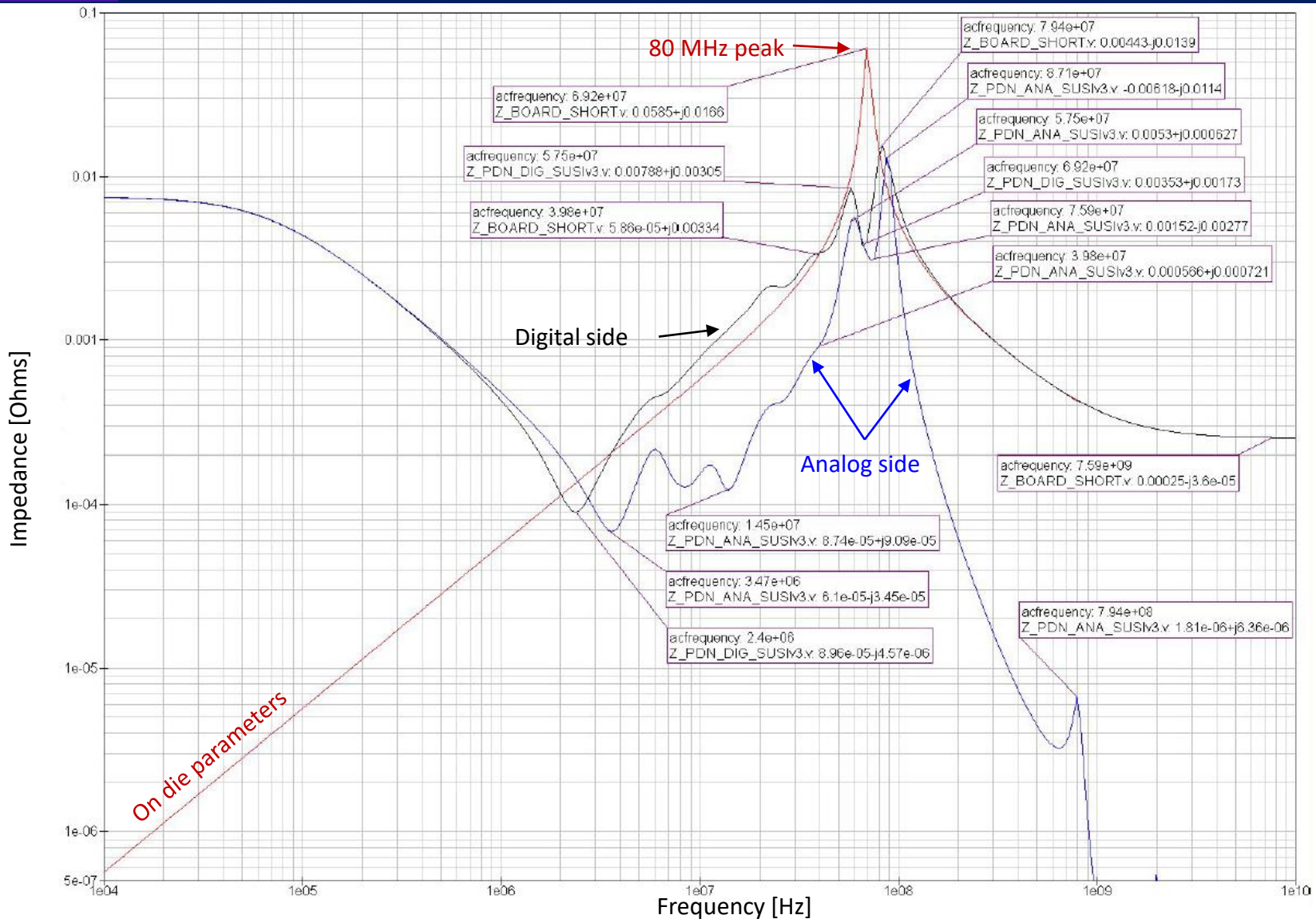
https://edms.cern.ch/file/2404958/1/WorkPackage_RELEASED_SUSI_v3.0.1_13-AUGUST-2020.zip

Common characteristics:

- Material: Low mass flexible circuit made by polyamide
- Power: low voltage @ +1.2V; high voltage @ +-500V, sense lines for low voltage regulation
- I2C, Reset, Clock and TFC @ 40MHz SLVS

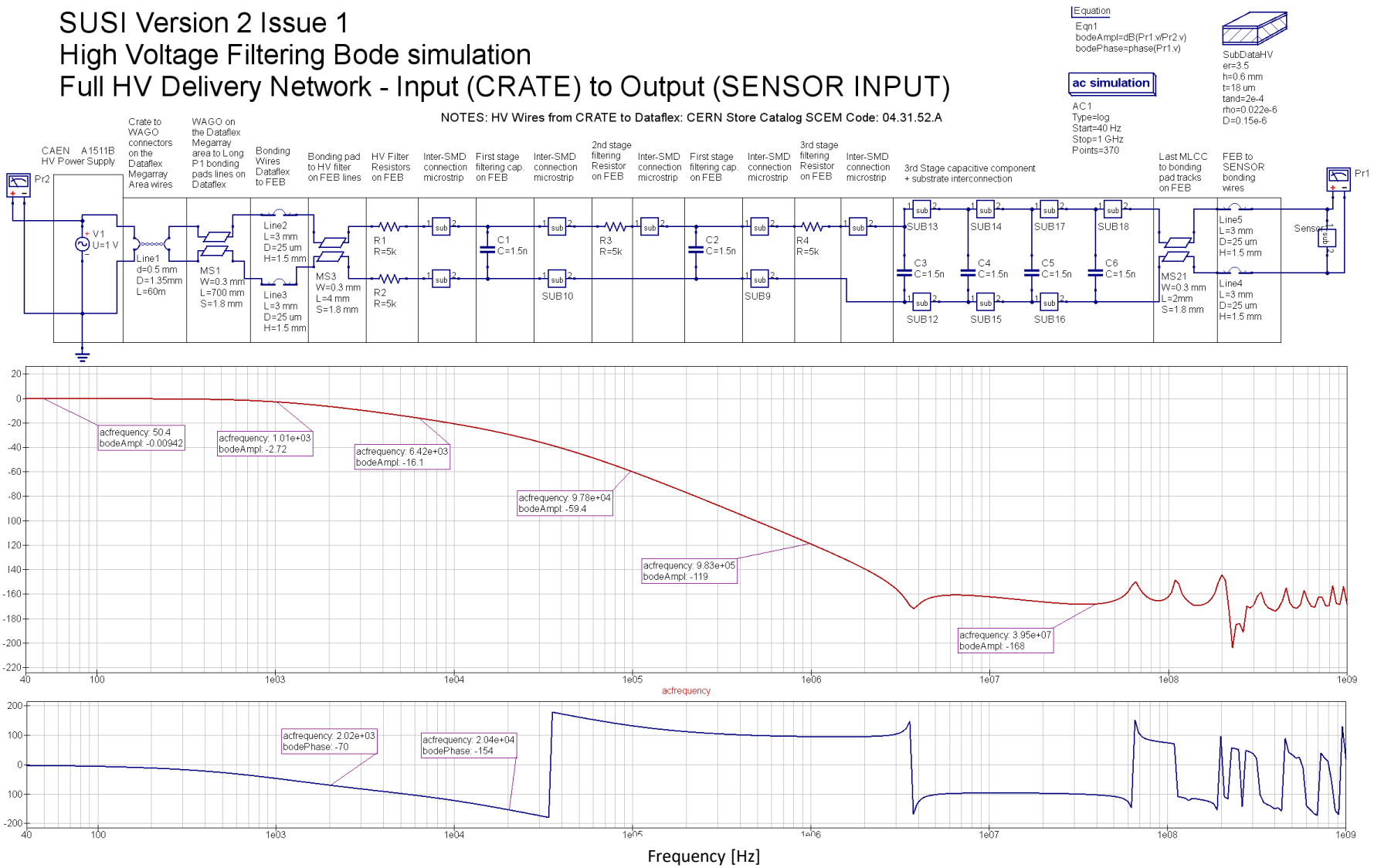
PDN optimized to improve PSRR in the range 40 MHz – 80 MHz

Hybrid Circuit Design – LV filter



Hybrid Circuit Design – HV filter

SUSI Version 2 Issue 1
High Voltage Filtering Bode simulation
Full HV Delivery Network - Input (CRATE) to Output (SENSOR INPUT)



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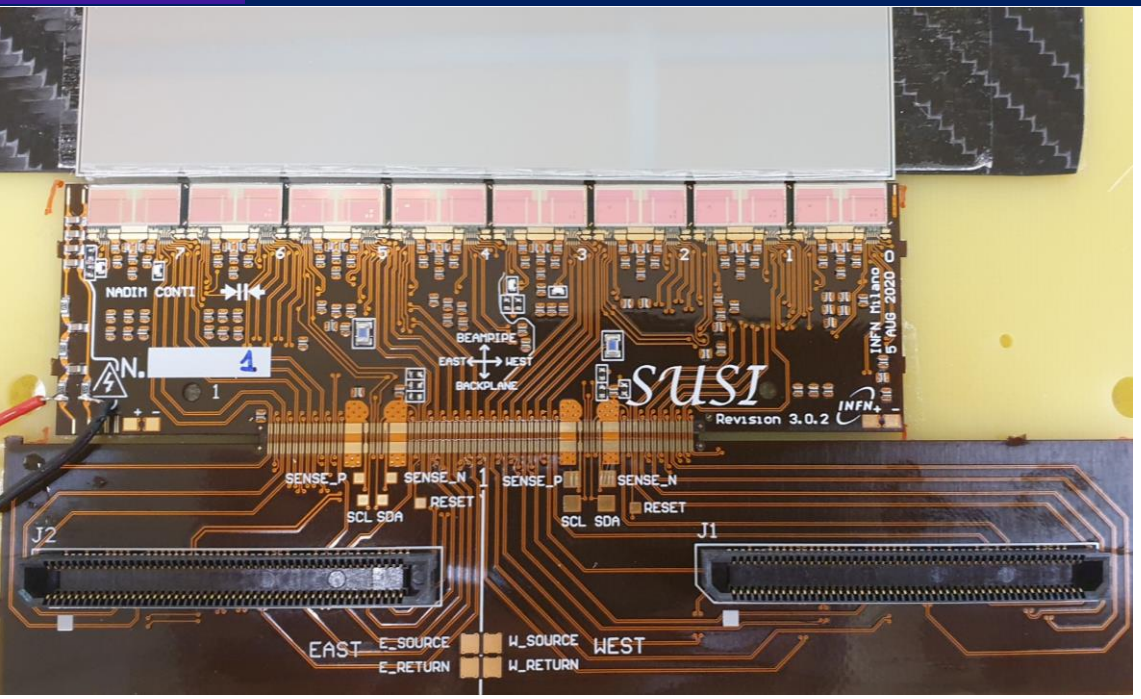
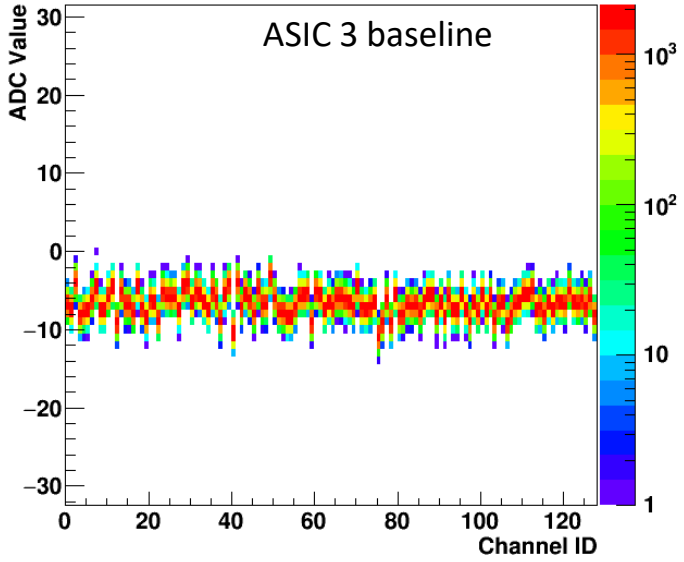
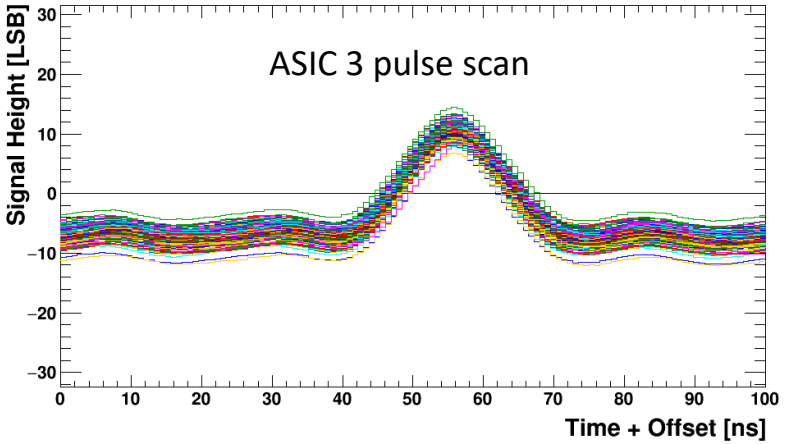
Prototype Test

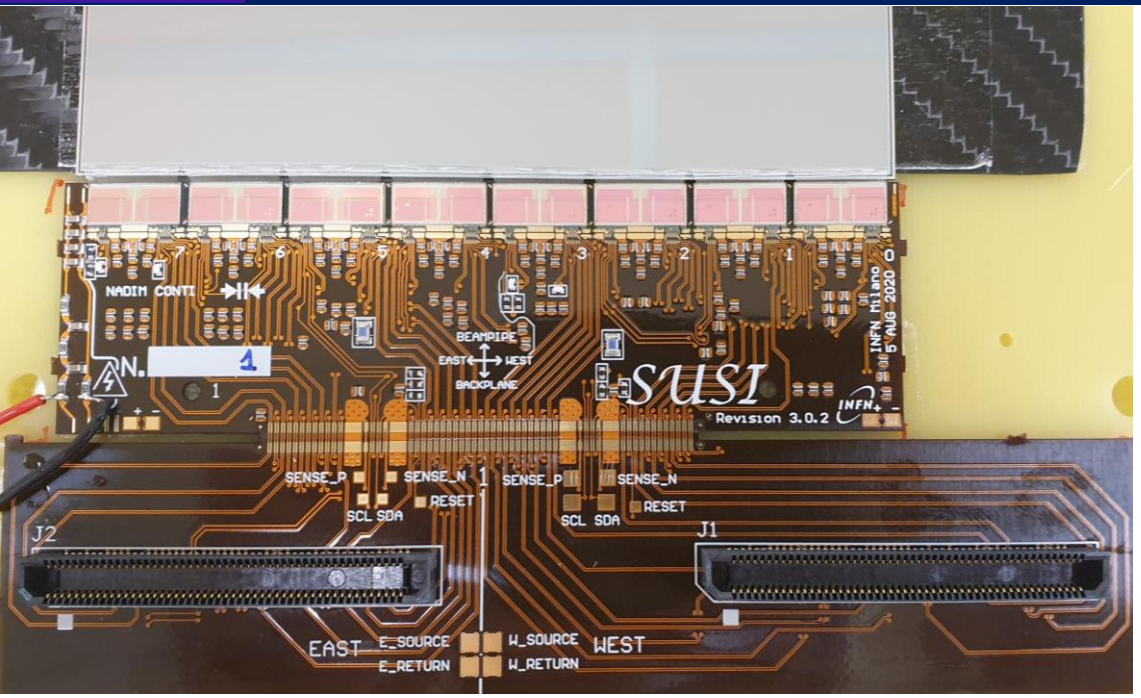


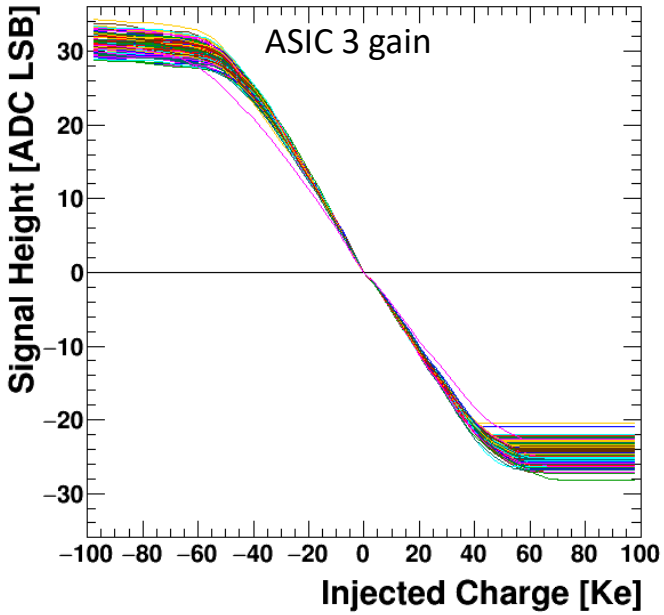


- Several test performed:
  - on VERA with type A biased sensor
  - on SUSI with type B biased sensor
- Both VERA and SUSI show:
  - Great noise performances < 1 LSB
  - Residual digital pickup at 40 MHz on pulse scan



Prototype Test





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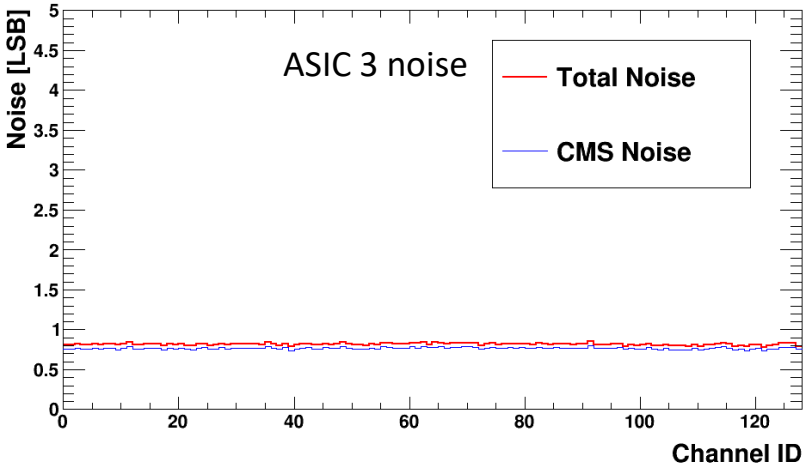
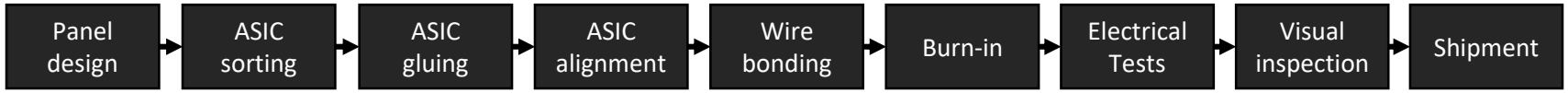


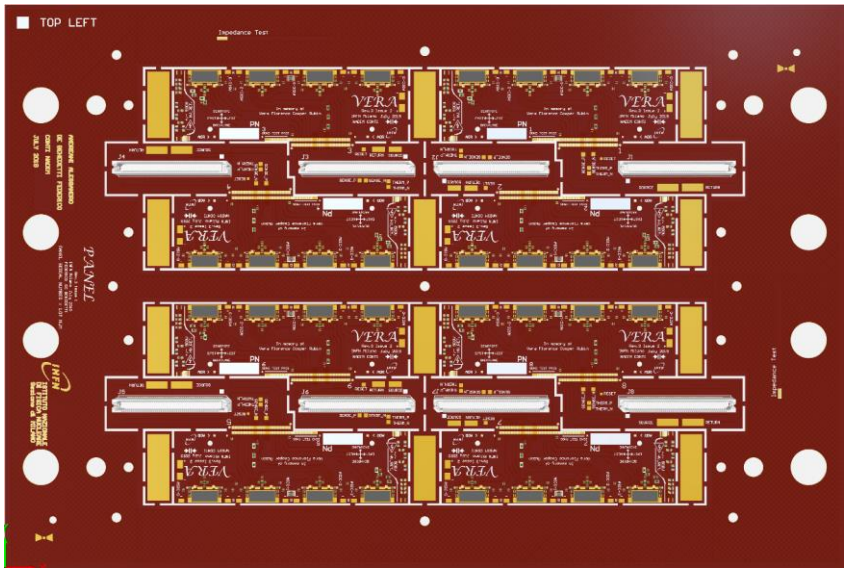
Hybrid Circuit Production

- Panel design
- ASIC sorting, gluing and alignment
- Wire bonding
- Burn-in test, hardware and software
- Electrical tests and grading
- Visual inspection and shipment

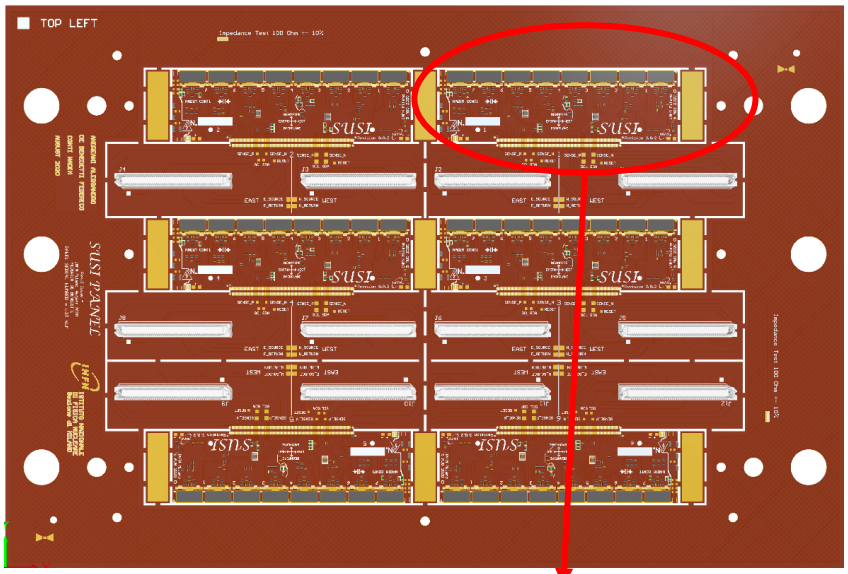


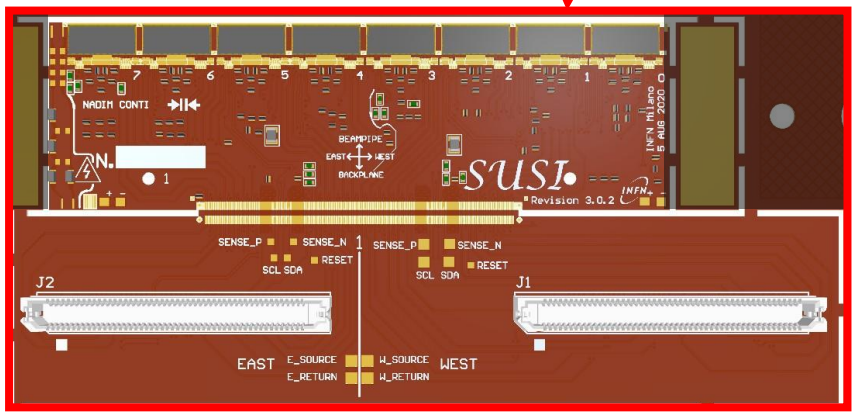
Hybrid Circuit Design - Panel

VERA Panel – 8 circuits (32 ASICs)



SUSI Panel – 6 circuits (48 ASICs)



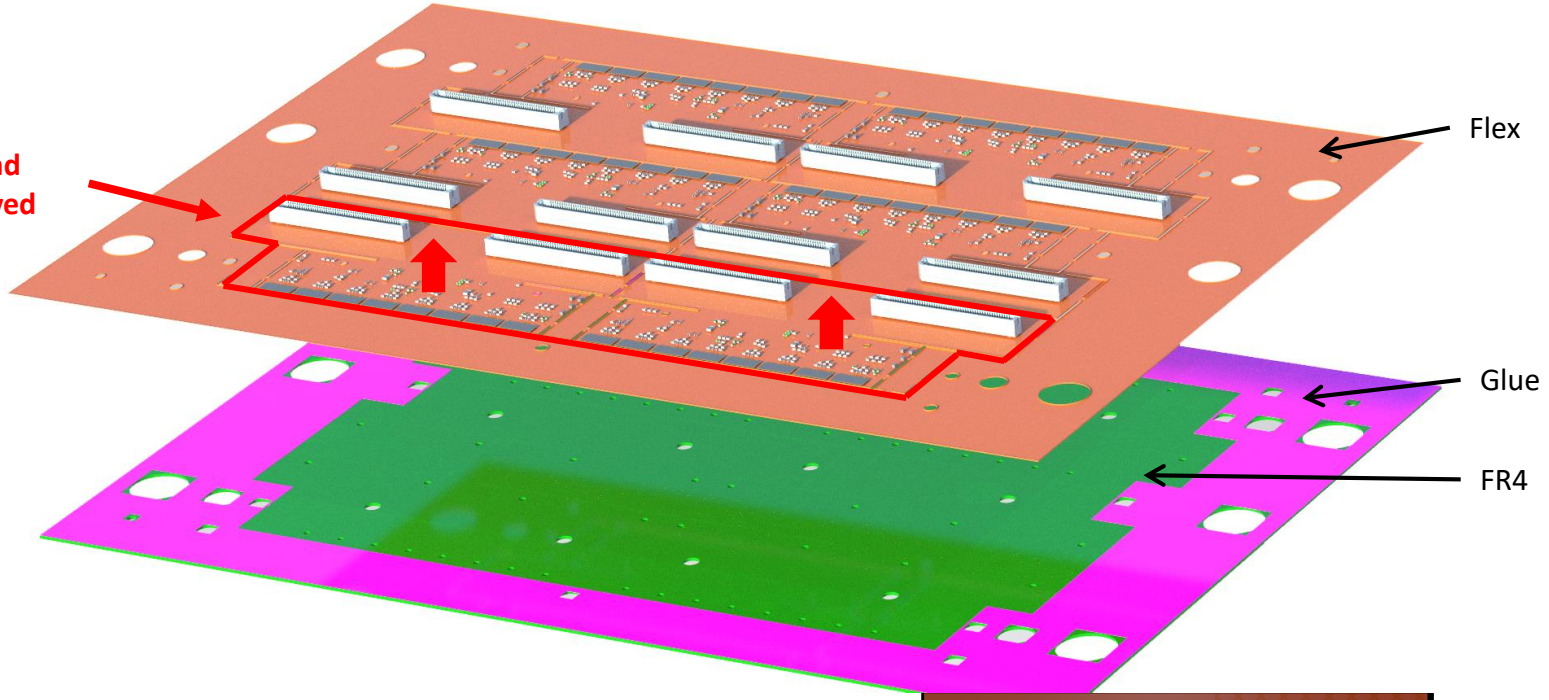


- Final hybrids are arranged in panels of 350x235 mm
- Aim to:
  - Reduce PCB fabrication costs, ASIC and wire bonding assembly time, module production
  - Testing the hybrids through a dedicated connector

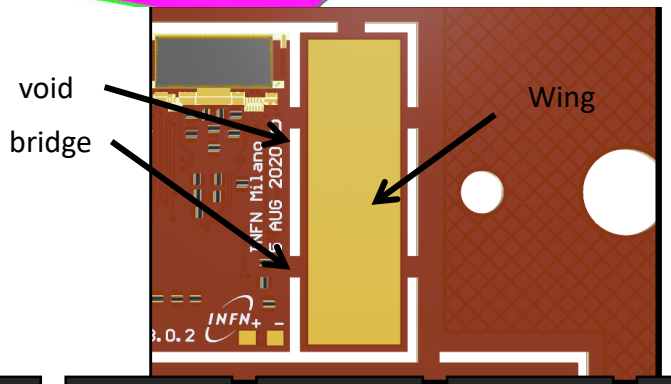
Single hybrid cutout for module production

Panel design → ASIC sorting → ASIC gluing → ASIC alignment → Wire bonding → Burn-in → Electrical Tests → Visual inspection → Shipment

Hybrid Circuit Design - Panel



- Added an FR4 back panel as rigidizer for production assembly
- Bridges and voids for easy cutout
- Added ENIG wings for manipulating the hybrid with a vacuum pickup tool
- Slip fit dowel holes for pickup tool alignment



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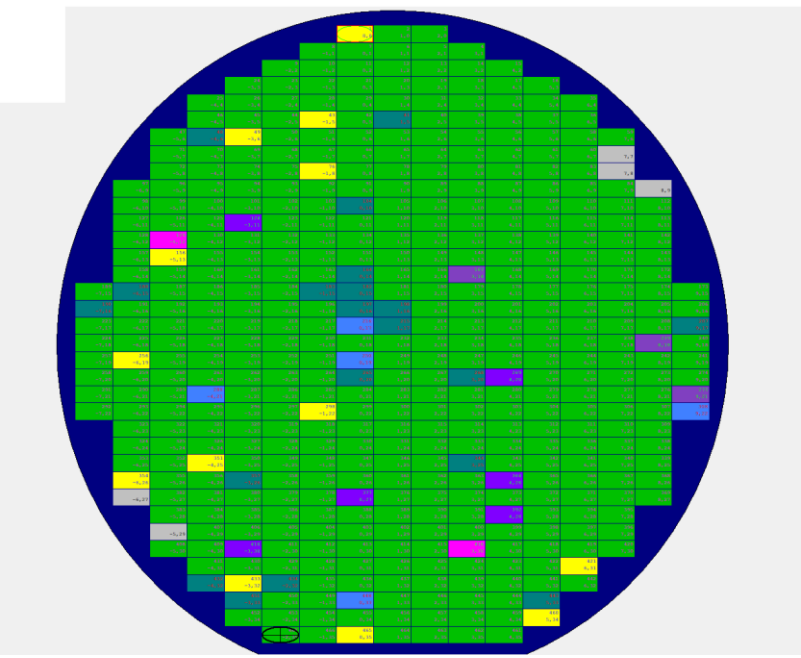
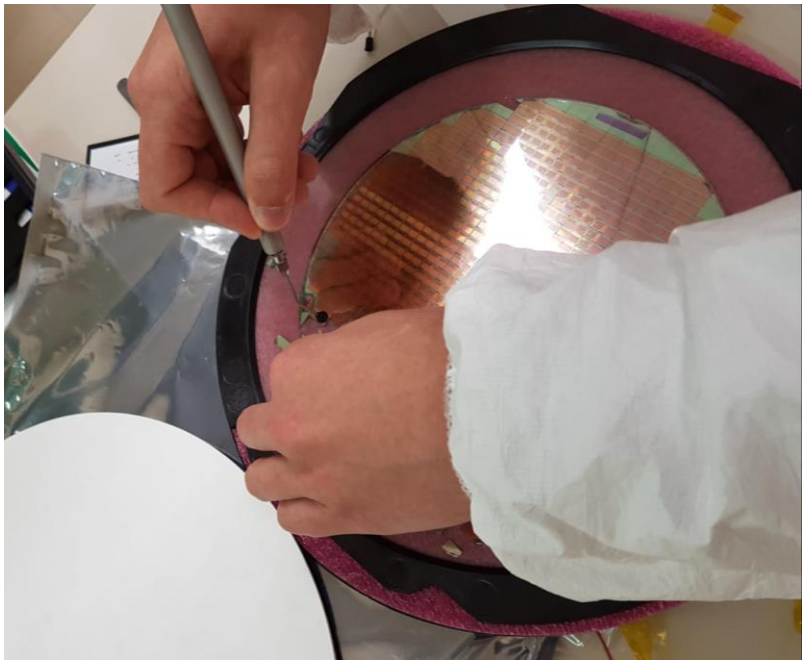
Production – ASIC Sorting

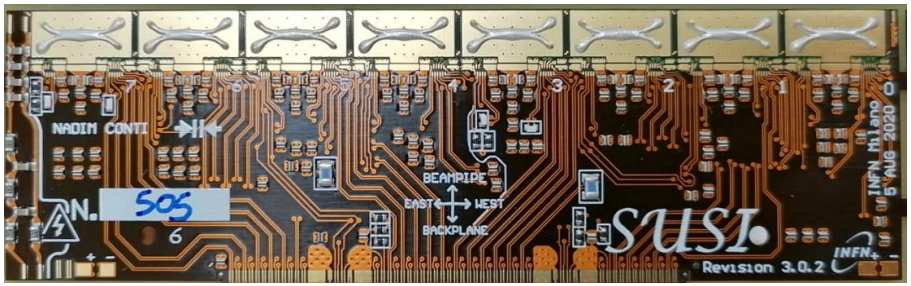


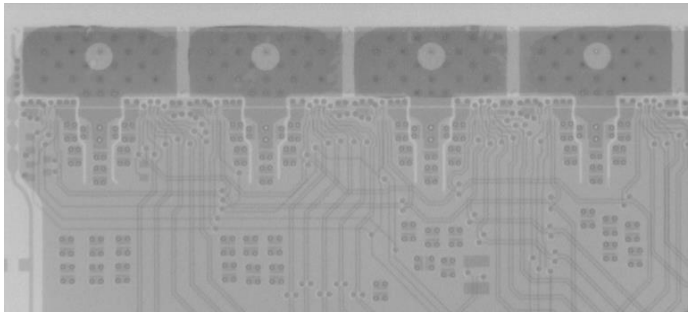


- Manual sorting done in Milan
- Wafer map with good/bad ASICs, provided by UZH
- More than 20 wafers (8000 ASICs) processed
- Yield 80%

Panel design → **ASIC sorting** → ASIC gluing → ASIC alignment → Wire bonding → Burn-in → Electrical Tests → Visual inspection → Shipment

Production – ASIC gluing

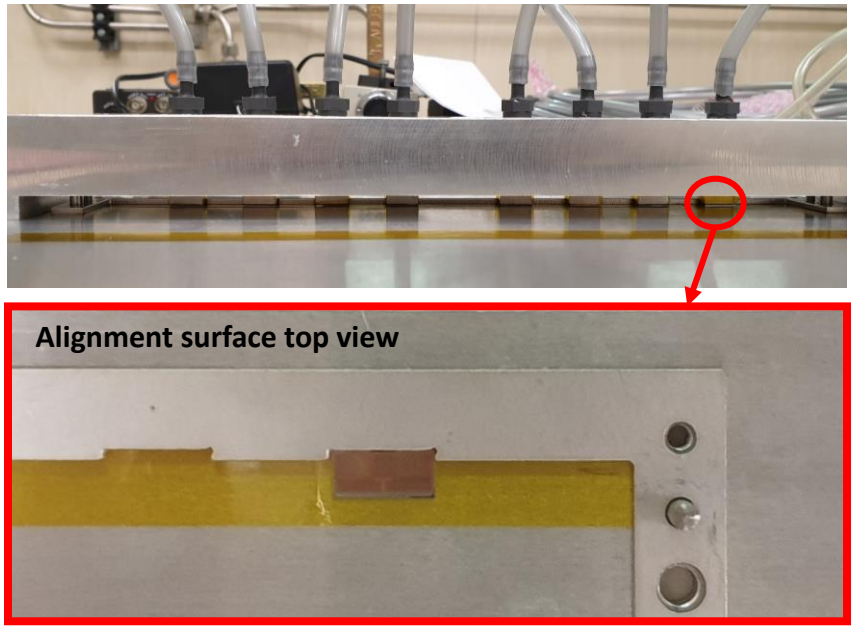


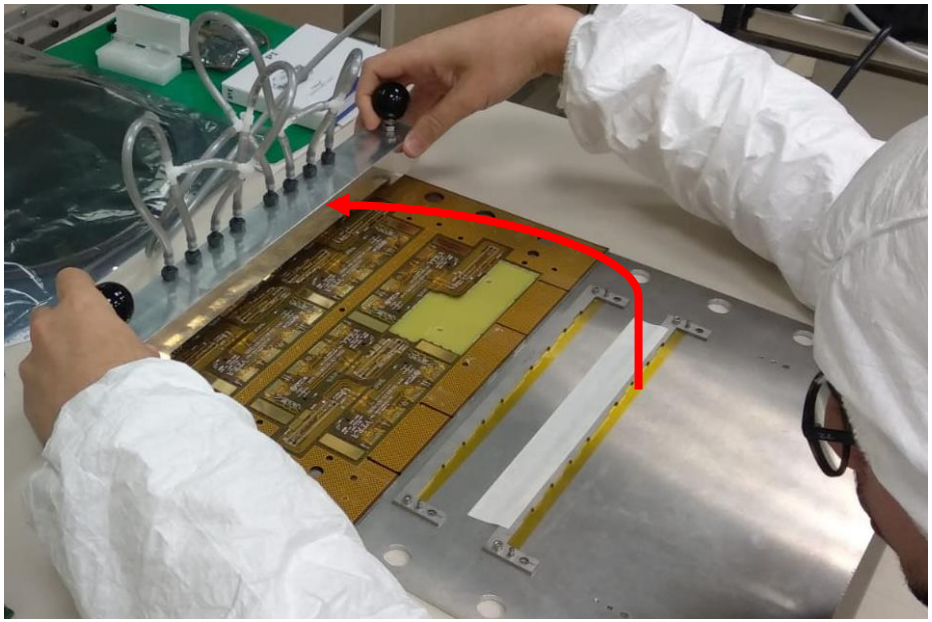


- LOCTITE ABLESTIK 2902, bi-component glue with silver
- Electrically and thermally conductive
  - Cooling pipe located under the ASICs
- Optimal glue pattern studied for maximum coverage with no glue spill
- X-Ray for qualification

Panel design → ASIC sorting → **ASIC gluing** → ASIC alignment → Wire bonding → Burn-in → Electrical Tests → Visual inspection → Shipment

Production – ASIC Alignment

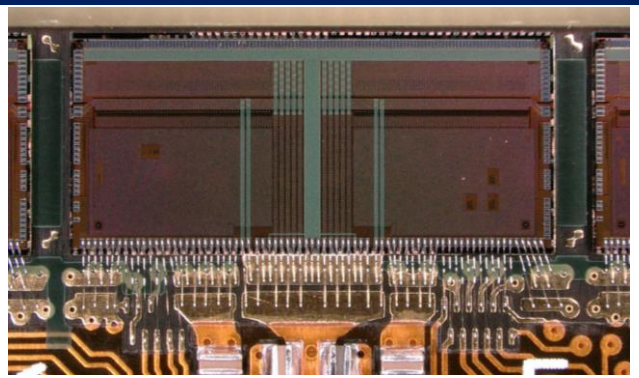


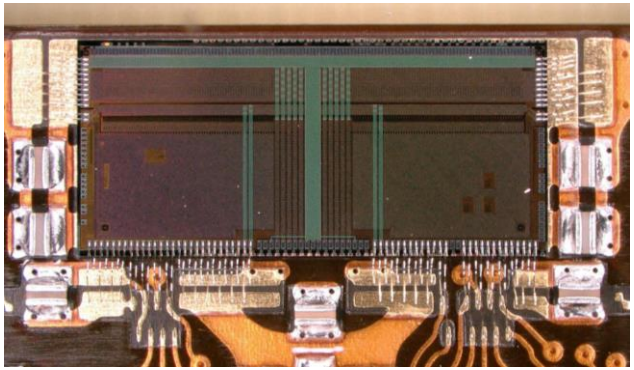


- VERA assembly done using a vacuum pick-up tool developed in Milan
  - ASICs transferred from an alignment surface to the panel
- SUSI assembly done with an automatic pick and place machine from an external company
- Curing at 25°C for 1 day

Panel design → ASIC sorting → ASIC gluing → **ASIC alignment** → Wire bonding → Burn-in → Electrical Tests → Visual inspection → Shipment

Production – Wire Bonding

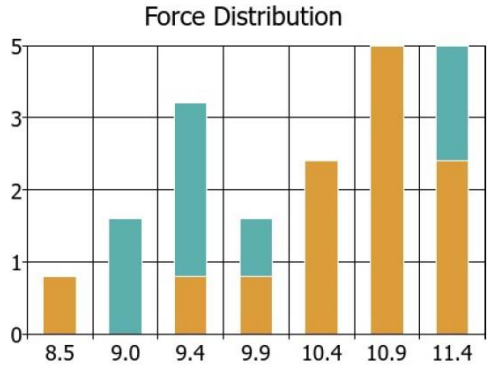


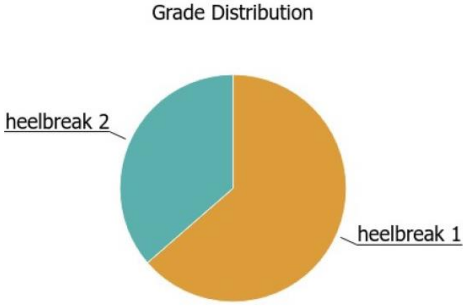


Statistics

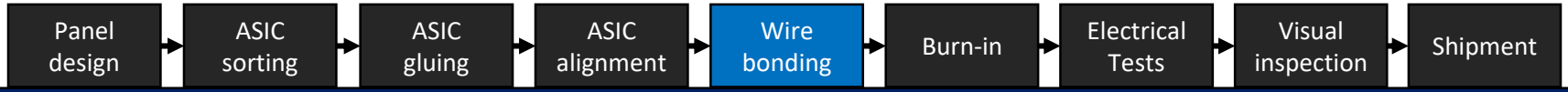
Min=8.2gram, Max=12.1gram, Mean=10.4gram
Count=22, Stdev=1.0

Cpk=2.5
(LSL=3.0gram)





- Wire bonding performed with Delvotec G4 6400
- Custom vacuum plates for holding the panel during the wire bond
- 99% Al + 1% Si 25 um diameter wire
- Two different wire disposition for VERA and SUSI hybrids
- Pull test for wire bonding qualification

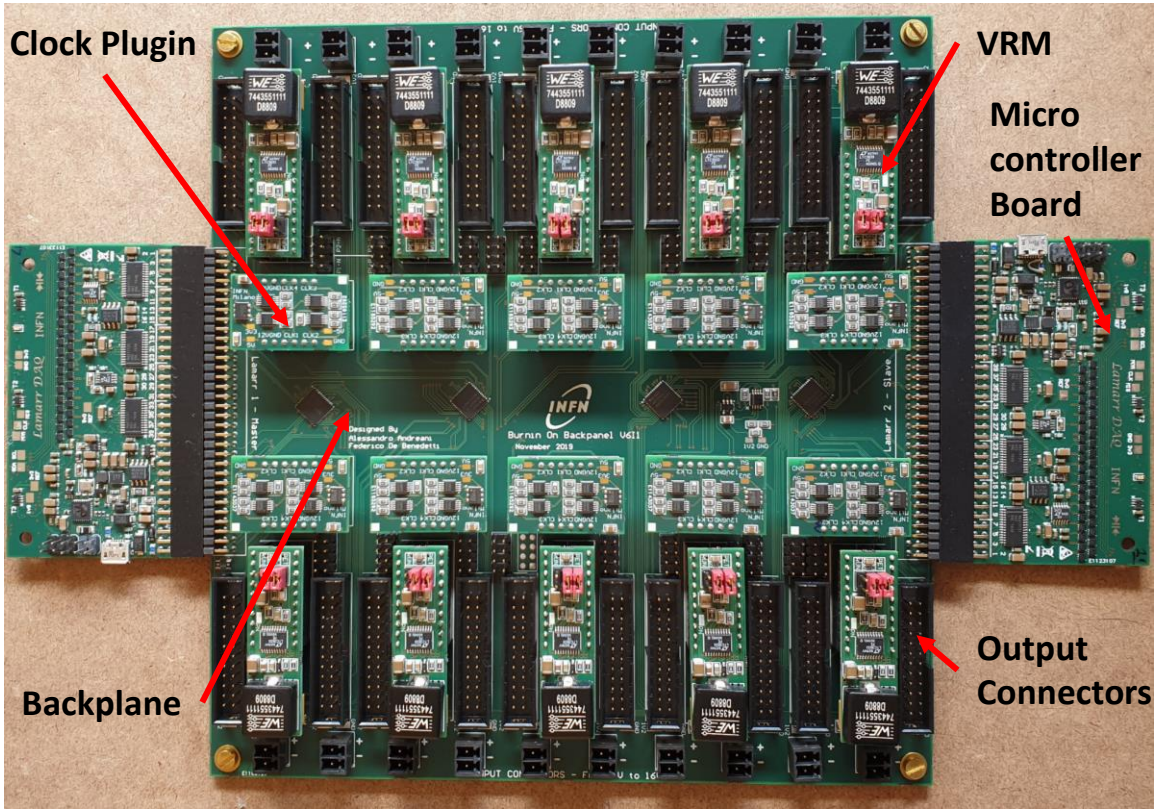


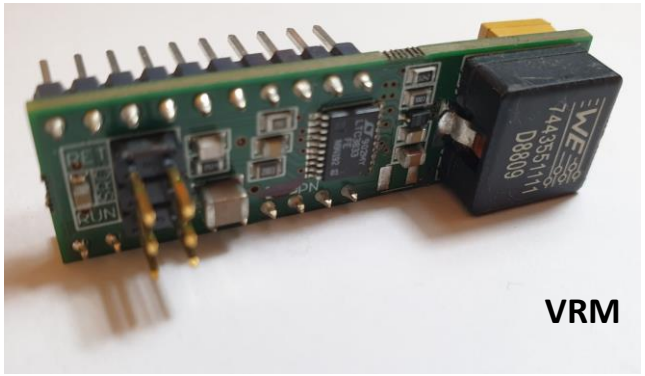
Production – Burn-in

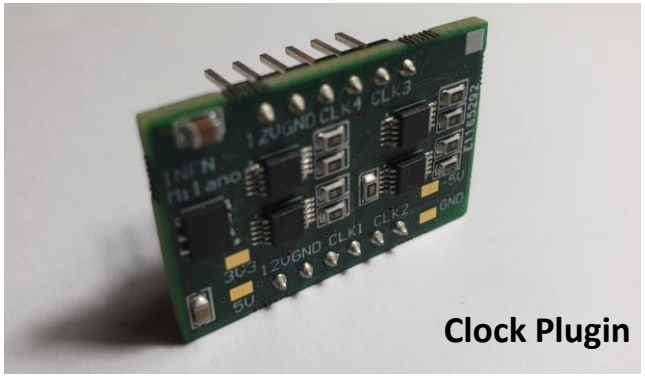
- **Burn-in is introduced to detect premature failures of the produced modules**
- 7 days of burn-in at 60°C, hybrids fully powered, clocked and programmed via I2C
- Temperature, humidity and I2C monitoring
- **Capable to perform burn-in up to 10 panels at a time**

Panel design → ASIC sorting → ASIC gluing → ASIC alignment → Wire bonding → **Burn-in** → Electrical Tests → Visual inspection → Shipment

Production - Burn-in Hardware



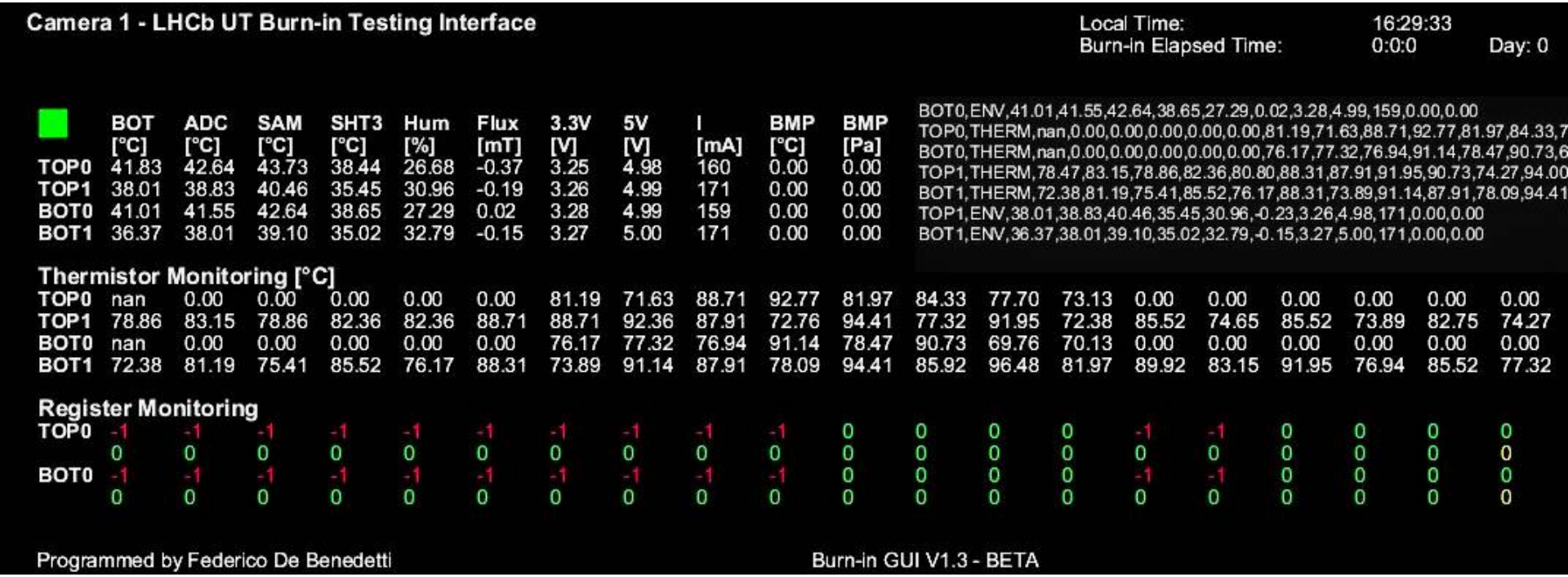




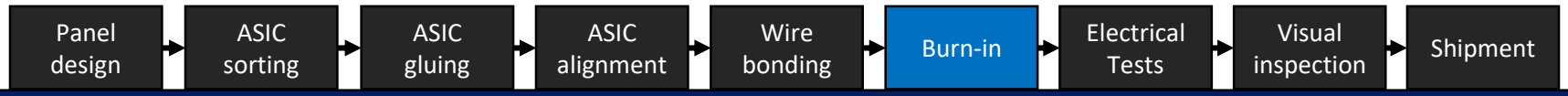
- **Voltage Regulator Module (VRM):** step down converter, custom design for 1.2V fine regulation with sense line.
- **Clock plugin:** 40 MHz SLVS buffer tree for clocking the hybrids.
- **Microcontroller board:** for burn-in monitoring and ASICs programming
- **Backplane:** I2C multiplexers

Panel design → ASIC sorting → ASIC gluing → ASIC alignment → Wire bonding → **Burn-in** → Electrical Tests → Visual inspection → Shipment

Production - Burn-in Software

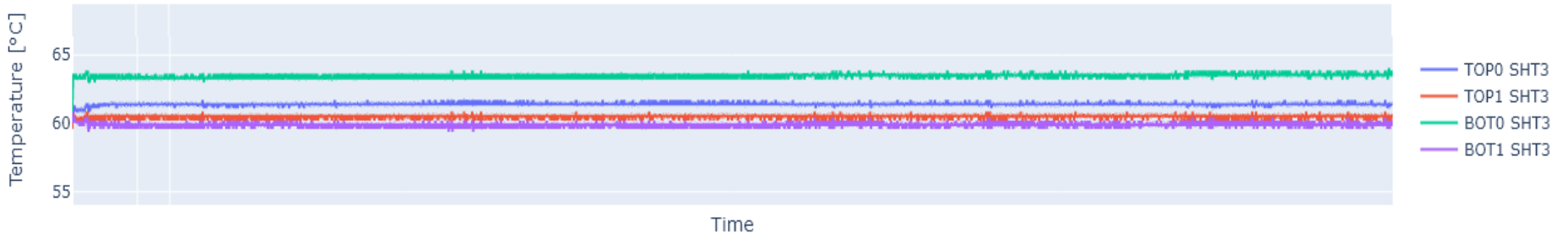


- **Java software for online monitoring**
- Log function for offline analisys

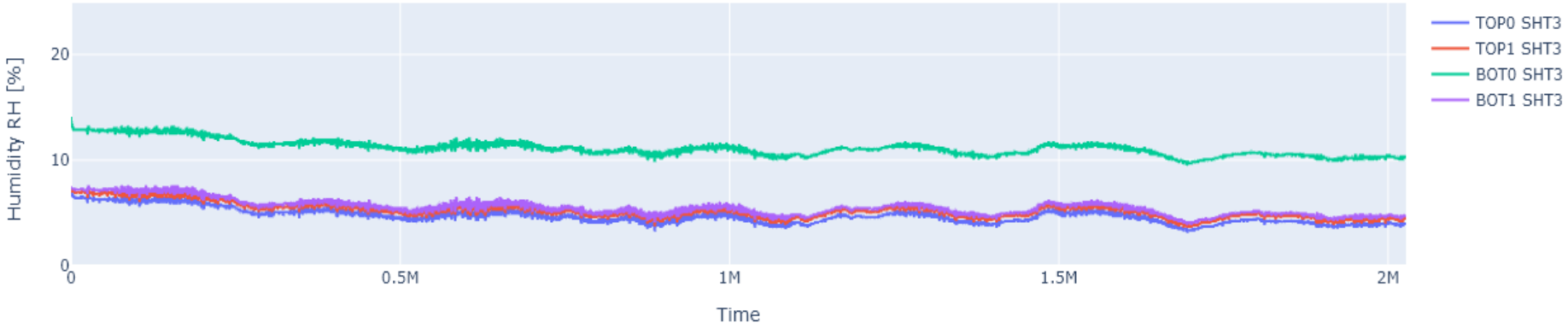


Production - Burn-in Software

Temperature monitoring



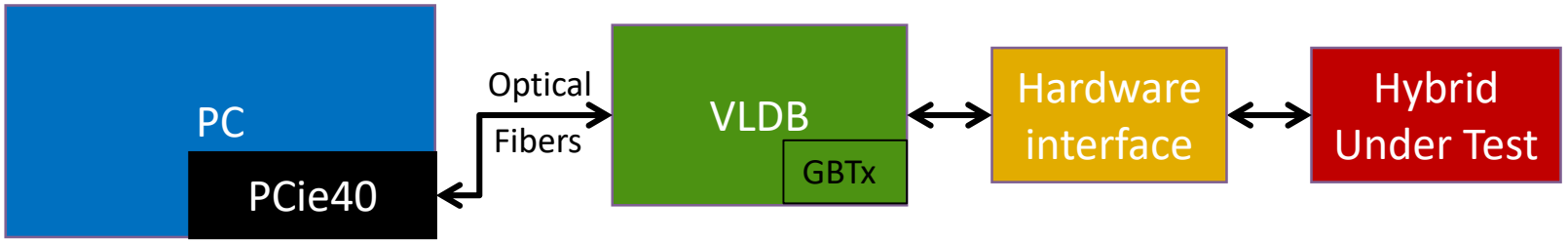
Humidity monitoring

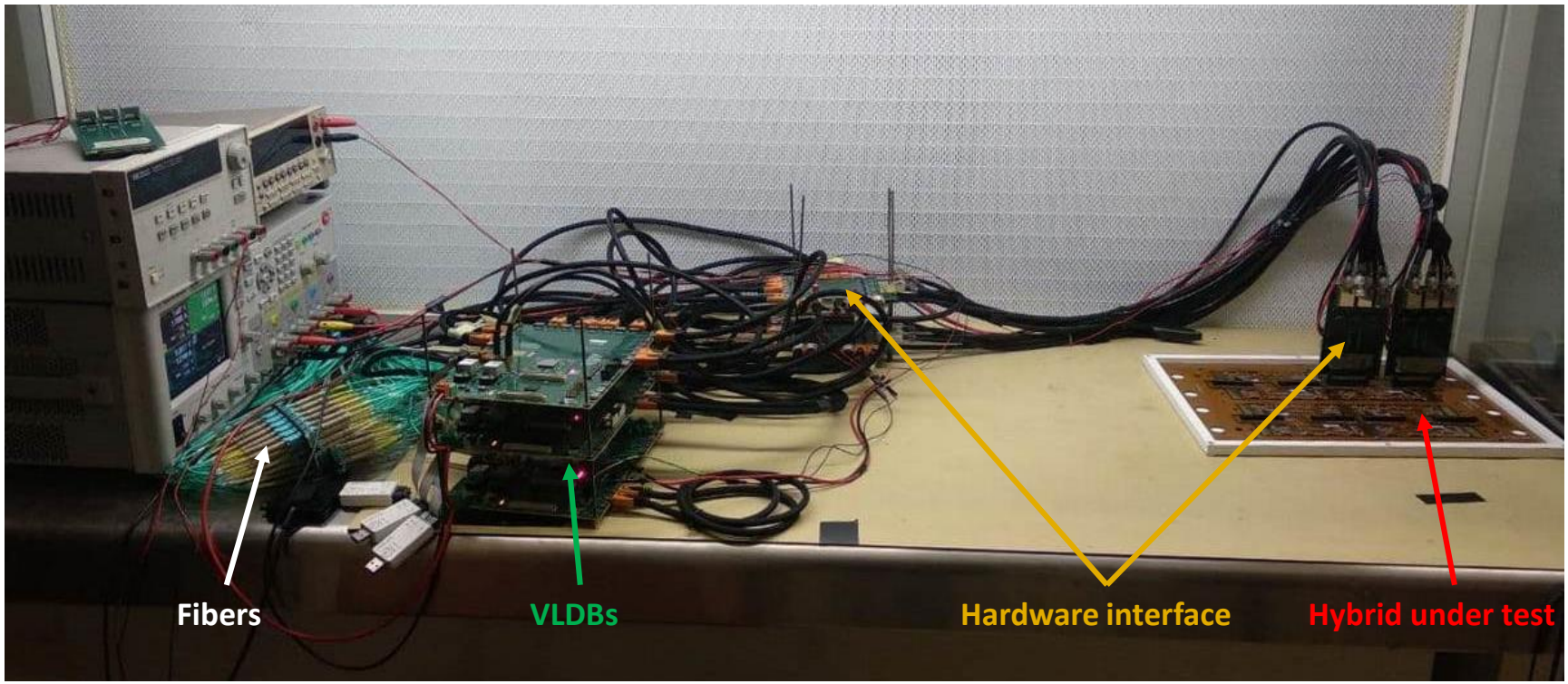


- Java software for online monitoring
- **Log function for offline analisys**

Panel design → ASIC sorting → ASIC gluing → ASIC alignment → Wire bonding → **Burn-in** → Electrical Tests → Visual inspection → Shipment

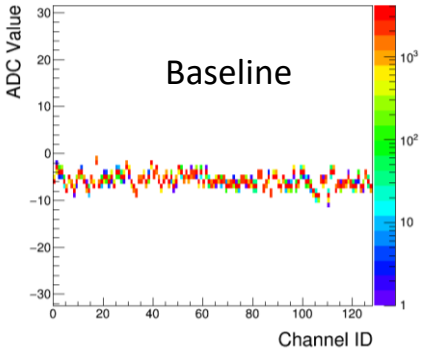
Production - Electrical Test Hardware

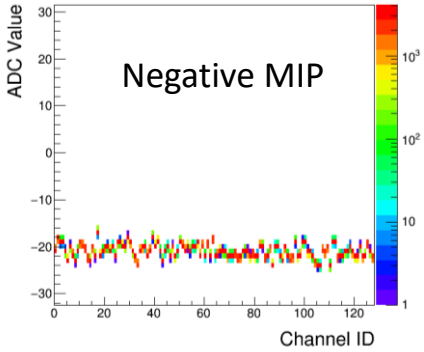


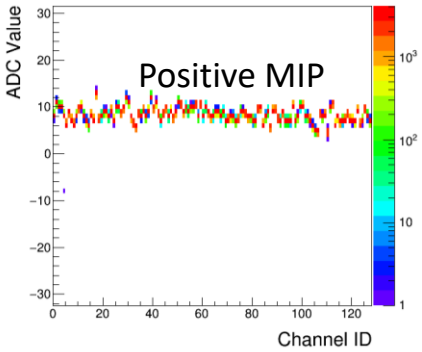


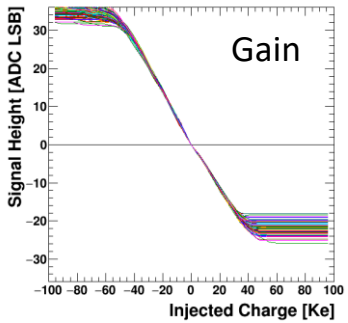
Panel design → ASIC sorting → ASIC gluing → ASIC alignment → Wire bonding → Burn-in → **Electrical Tests** → Visual inspection → Shipment

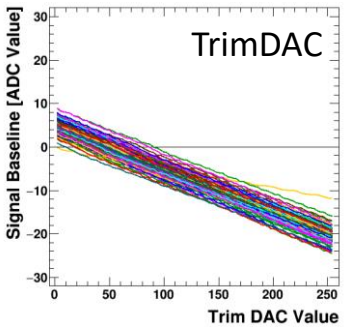
Production - Electrical Test Plots

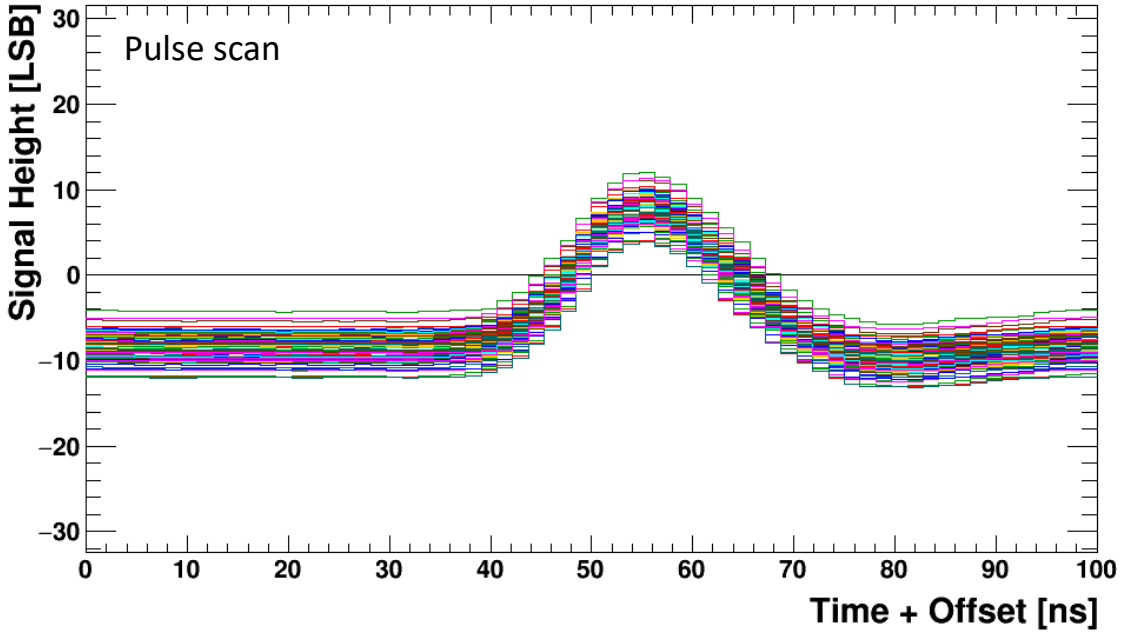












Panel design → ASIC sorting → ASIC gluing → ASIC alignment → Wire bonding → Burn-in → **Electrical Tests** → Visual inspection → Shipment

Production - Electrical Test Grading

- Automatic report of electrical test is generated

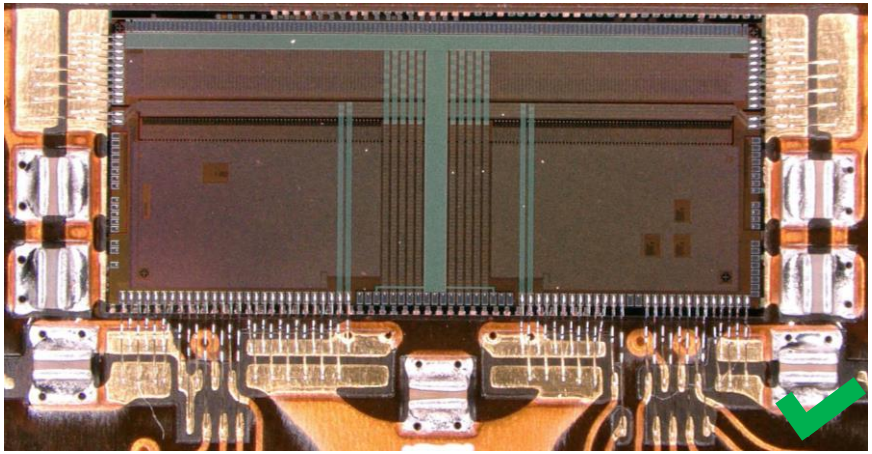
```
--------------------------------------------------------------------------------
AUTOMATIC SUMMARY OF PROBLEMATIC CHANNELS for
PANEL185_AFTER-HYBRID8
--------------------------------------------------------------------------------
Noisy channels (RMS>3) BASELINE   :
Noisy channels (RMS>3) NEG INJECT :
Noisy channels (RMS>3) POS INJECT :
--------------------------------------------------------------------------------
BASELINE Outliers |base-mean|<7   :
--------------------------------------------------------------------------------
Saturating BASELINE (modulus<29)  :
Saturating NEG INJECT (modulus<29):
Saturating POS INJECT (modulus<29):
Low Gain (GAIN<10 ADC/mip)        :
--------------------------------------------------------------------------------
STATISTICS OF TrimDAC CURVE
Number of channels : 512.0
-----------------------
Intercept mean gaussian  7.35
Intercept sigma gaussian  1.71
Slope mean gaussian  -0.0991
Slope sigma gaussian   0.0050
-----------------------
Channels outside 5 sigmas of the intercept

Channels outside 5 sigmas of the slope

-----------------------
```

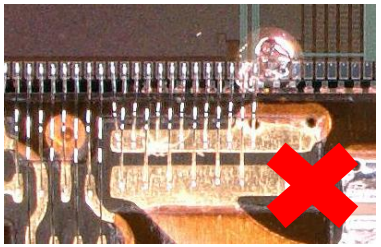
- The hybrid is graded accordingly to the table, then uploaded to the official database

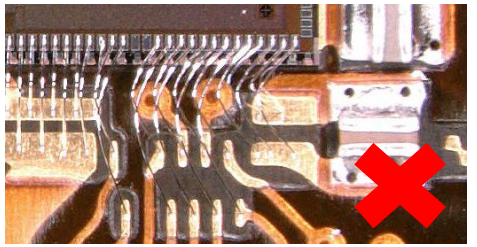
Grade	Problematic Channels
A+	0
A	1
A-	2
B+	3
B	4
B-	5
D	>5
F	Mechanical failure or short circuit

Panel design → ASIC sorting → ASIC gluing → ASIC alignment → Wire bonding → Burn-in → **Electrical Tests** → Visual inspection → Shipment

Production - Visual Inspection



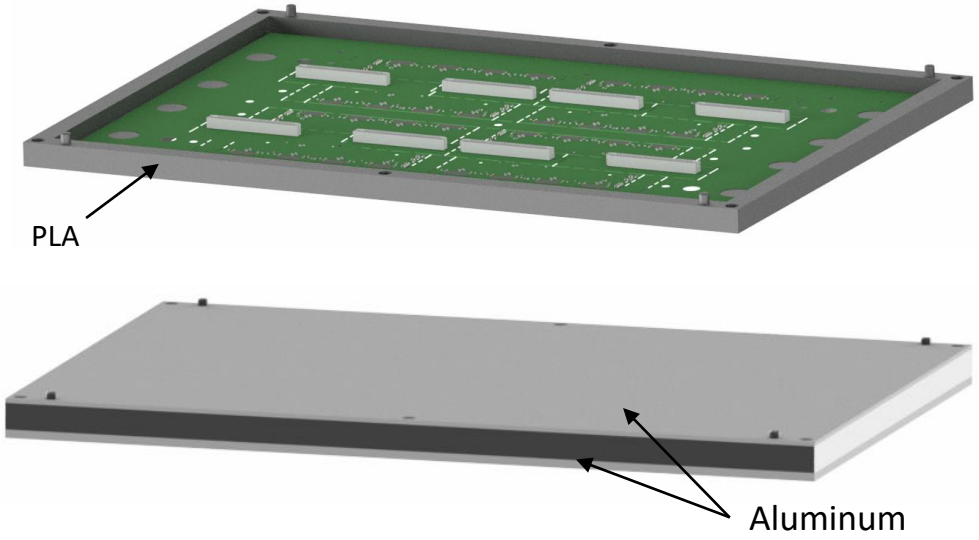




- Final optical inspection to detect mechanical problems as: scratches on pads, damaged wire bonds, damaged hybrids…..

Panel design → ASIC sorting → ASIC gluing → ASIC alignment → Wire bonding → Burn-in → Electrical Tests → **Visual inspection** → Shipment

Production - Shipment



- All the panels produced in Milano were shipped to Syracuse University (NY)
- Custom transport box developed for the panel
  - PLA 3D printed frame
  - Top and bottom aluminum plates
  - Stackable design
- Vacuum bag to protect the electronics against moisture
- **No damaged wire bonds due to the shipment**

Panel design → ASIC sorting → ASIC gluing → ASIC alignment → Wire bonding → Burn-in → Electrical Tests → Visual inspection → Shipment

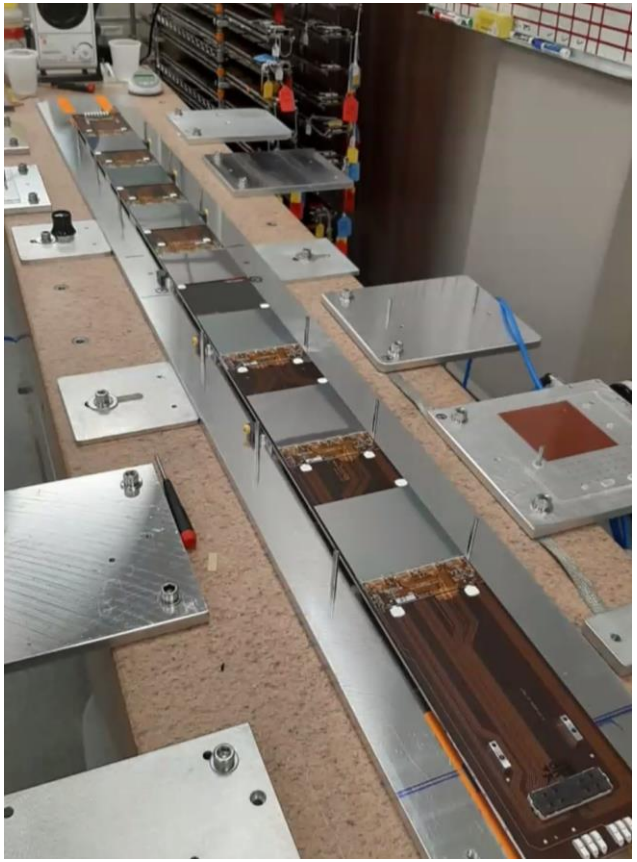
Summary

Hybrid production:

- 1080 VERA hybrids and 110 SUSI hybrids assembled and tested
- All the hybrids shipped to Syracuse University (NY) for stave assembly

Stave production:

- Module costruction for UT core done, spare module ongoing
- Stave construction is ongoing
- 25 fully instrumented stave at CERN + 5 stave ready for shipment
- All the stave flavours (A,B,C) have been produced



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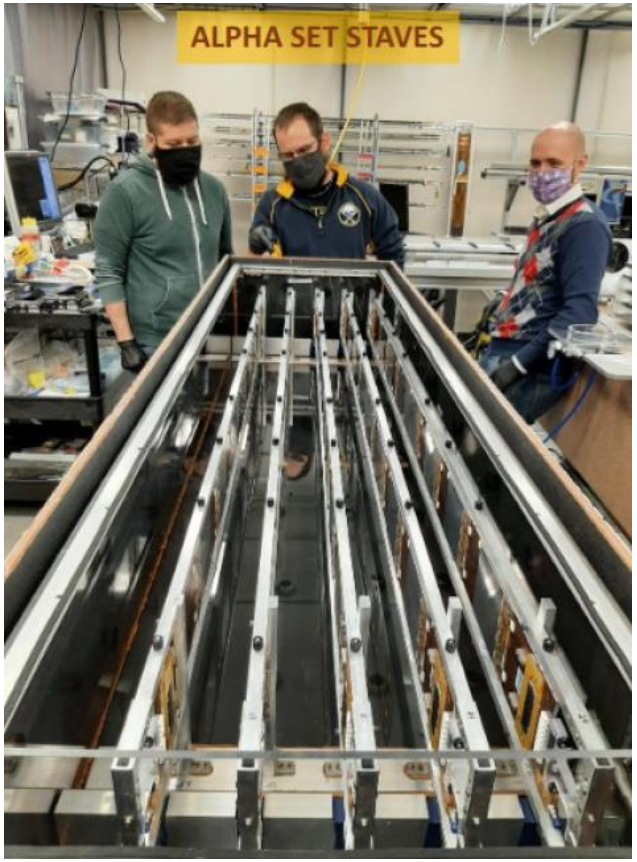
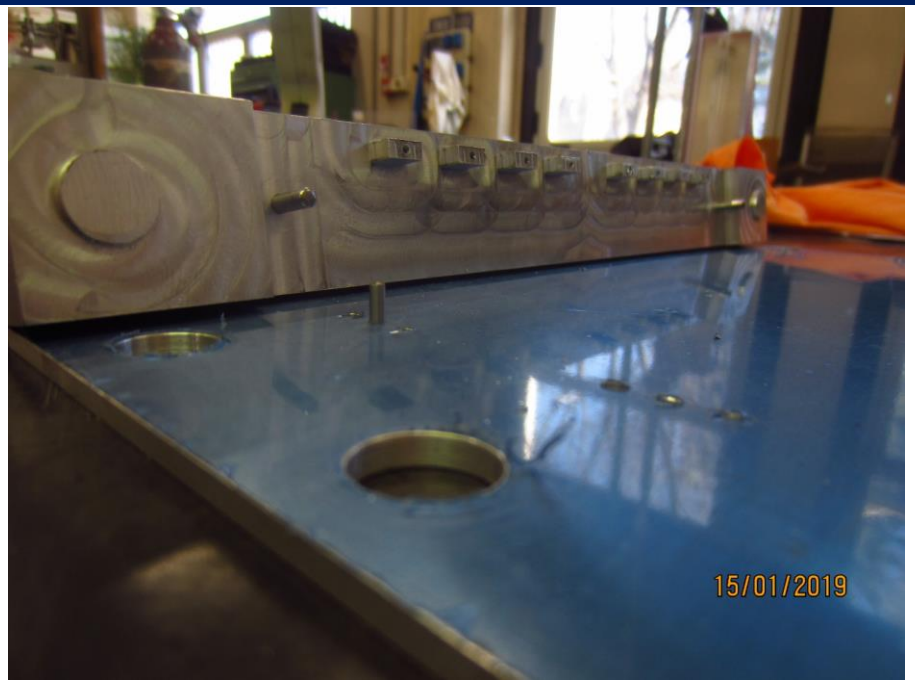
Detector plans:

- Start final stave test at CERN by November 2021
- **Aiming to finish the installation underground by February 2022**



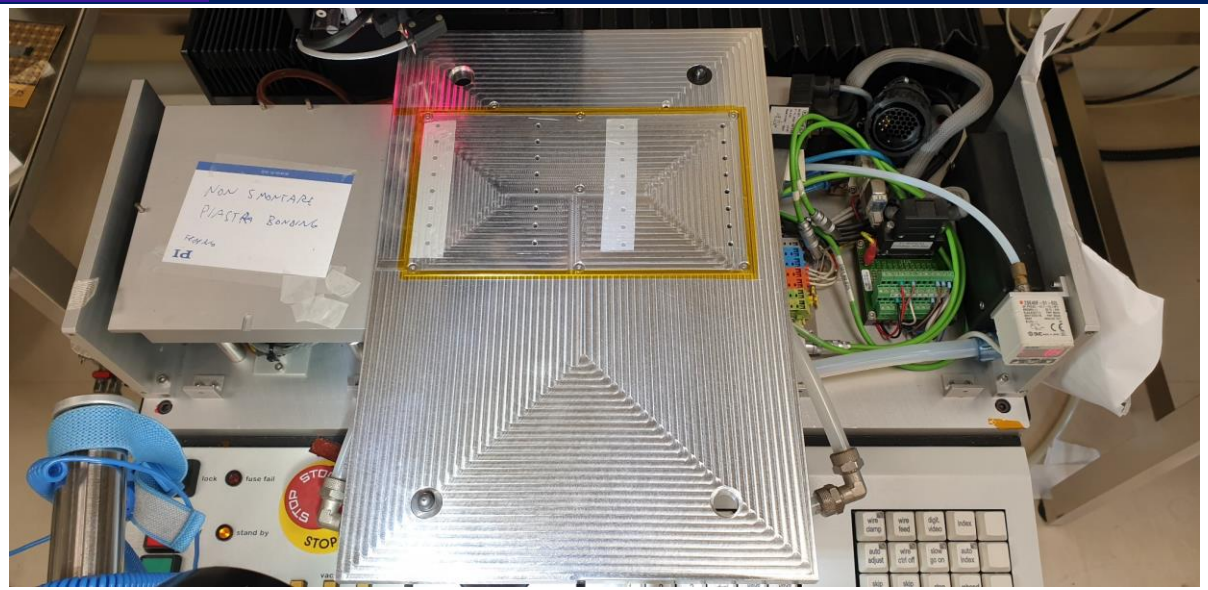
Backup Slides

Tools for Hybrid Production



- Pfeiffer vacuum pump used during production, for ASIC alignment and panel gluing
- Pickup tool for VERA ASIC alignment

Tools for Hybrid Production



- Custom vacuum plates designed for holding the panel on the wire bonder and the glue robot