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Augmenting Quality and Throughput of Functional Testing and Device Characterization for the ABCStar ATLAS-ITk Strips Readout ASIC Through a Semiconductor Test Industry Partnership

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To instrument the 60 million ATLAS ITk Strips Sensor channels, CERN developed the mixed-signal ABCStar front-end readout ASIC. Over 350,000 devices on 753 wafers containing 466 ASICs each will be extensively tested to provide the chips required for sensor modules. Carleton achieved a 3-10 times improvement in throughput, without compromising test coverage or data collection, by developing new tools and techniques in partnership with a specialist wafer testing company –jointly overcoming the methodological, technical, and semantic divides that exist between physics laboratories and the semiconductor test industry, and opening new possibilities in ASIC testing for future particle physics projects.

Summary (500 words)

The Department of Physics at Carleton University has a venerable history of involvement in detector conceptualization, design, construction, and testing. Due to the growing prevalence of Application Specific Integrated Circuits (ASICs) in experiments of all scales –and an identified need for more capacity around all aspects of their design, production, and testing –in 2015 we undertook to gain the required expertise to test unpackaged ASICs at the wafer level as part of the Canadian contribution to the silicon-strips portion of the new ATLAS Inner Tracker (ITk) for the HL-LHC.

ASICs for particle physics have traditionally been tested at academic or government facilities that allow for extensive research and experimentation, and where generous access to human resources and bespoke equipment is the norm. While many of these ASICs were of exceptional complexity and presented immense difficulties to test, the semiconductor testing industry is routinely dealing with far more challenging designs than those being used in, for instance, ITk. Rather than duplicating existing approaches, we partnered with a specialist ASIC testing company to leverage their expertise and infrastructure with the intent of achieving significant improvements in wafer testing capabilities and throughput, and shorter test engineering and implementation cycles, while learning how to navigate the constraints inherently imposed by such a service-oriented commercial-industrial environment. We achieved a 3-10 times improvement in throughput over existing approaches, without compromising test coverage or data collection, by developing new tools and techniques with our industry partner –jointly overcoming the methodological, technical, and semantic divides that exist between our laboratories and the semiconductor test industry, and opening new possibilities in ASIC testing for future particle physics projects.

In 2018, we successfully tested our first ITk silicon-strips ABC130 interim front-end readout ASIC wafer using tests reverse-engineered from the ITSDAQ system –that we translated into custom C++ test software and stimulus vectors for the industry standard Advantest Smart Scale V93000 automated wafer test system. For the much-enhanced next generation ABCStarV0 readout chip in 2019, we started from scratch with the test requirements and the ASIC design specification to create a comparable test suite of our own that leveraged what we learned from the ABC130 and the capabilities and limitations of the V93000. Notably, we developed a macro compiler to generate test vectors and C++ code from assembler-like commands for direct import into the Advantest system, leveraged an advanced tester technique called Digital Source dynamic vectors to improve performance by an order of magnitude, and were able to "port"the Verilog validation tests from the ASIC simulation environment to the Avantest system using Cadence Xcelium. In 2020, we received ABCStarV1 wafers and adapted and enhanced our test suite as part of the pre-production phase.

Over 350,000 devices on 753 wafers containing 466 ASICs each need to be extensively tested before they are diced to provide high confidence the chips used for sensor module assembly are in compliance with all design specifications. Carleton and DA-Integrated have committed to test half of these wafers over two years.

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