Contribution ID: **113** Type: **Oral**

The lpGBT production testing system

Friday 24 September 2021 16:20 (16 minutes)

The Low-Power Gigabit Transceiver (lpGBT) is a radiation-tolerant ASIC designed to implement multipurpose high-speed bidirectional serial links in HEP experiments. Having more than 320 programmable registers, the ASIC is highly configurable. Its test must cover a large variety of functionalities which will be validated at three different power-supply voltages, two temperatures and over more than 1000 parameters. As more than 175 000 chips will be produced, optimizing the test duration is also a strong requirement. In this talk, an overview of the lpGBT v1 production test system will be given, challenges will be presented, and performance will be discussed.

Summary (500 words)

The Low-Power Gigabit Transceiver (lpGBT) is a radiation-tolerant ASIC designed to implement multipurpose high-speed bidirectional serial links in HEP experiments. Being data agnostic, it is typically used as the interface between the on-detector and off-detector electronics. It has a highly flexible front-end interface, supporting multiple serial links with configurable data rates for downlink and uplink data streams and also providing slow control features. Having more than 320 configurable registers and 11 configuration pins, the ASIC also provides a large number of programmable options to enable its efficient use in a wide variety of front-end applications. A new version of the ASIC, the lpGBT V1 is being produced to be installed in the experiments. More than 175 000 components will be distributed amongst the users.
The first testing phase will start in Q4 2021. More than 18 000 devices will be individually tested in order to deliver only devices that meet specific criteria based on their performance. The full production lot will be launched immediately after this first batch is tested and will be completed in Q4 2022.
The lpGBT tester runs up to 17 checkers to validate the device functionality. These tests cover all the chip's interfaces and features including high-speed links, PLLs, digital circuits as well as analog blocks such as ADCs and DACs. Additionally, to check all corners, the full test will be performed at three different power-supplies voltages, at -30℃ and at room temperatures. More than 1000 parameters will be measured per chip. Due to the number of components and the complexity of the test, one of the biggest challenges is to minimize the running time while maximizing the coverage.
To achieve this requirement, a specific test environment has been designed allowing the exchange of data and control signals between a Xilinx Virtex-7 FPGA VC707 Evaluation Kit, a custom lpGBT mezzanine board and a sophisticated test software. Finally, the test procedure is controlled via a general-purpose system developed at CERN, handling Graphical User Interface, data storage and postmortem analysis. The complexity of the tester also implied to use the state-of-the-art versioning tool, GitLAB, and a big part of the functionality it provides.
In this talk, an overview of the lpGBT v1 production test system will be given, the development process and the challenges will be presented, and performance will be discussed.

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Session Classification: Production, Testing and Reliability

Track Classification: Production, Testing and Reliability