TWEPP 2021

Topical Workshop on Electronics for Particle Physics (20-24 September 2021)

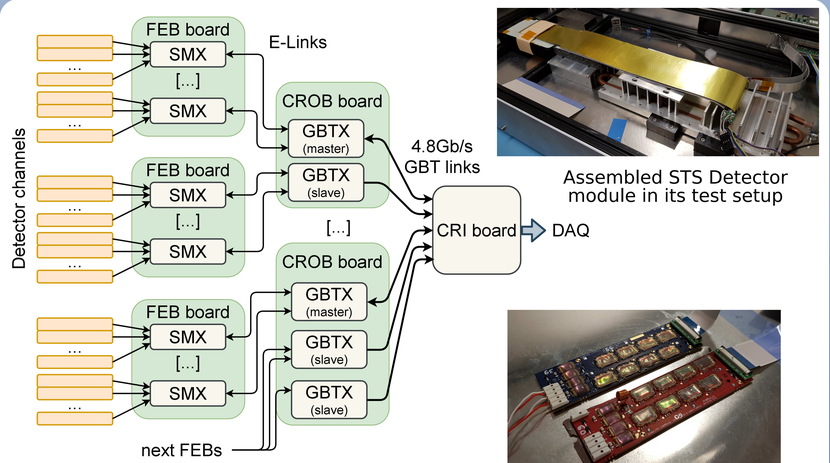
SMX and front-end board tester for CBM readout chain

Wojciech M. Zabołotny[1], David Emschermann[2], Marek Gumiński[1], Michał Kruszewski[1], Jörg Lehnert[2],Piotr Miedzik[1], Krzysztof Poźniak[1], Ryszard Romaniuk[1], Christian J. Schmidt[2]

[1]Institute of Electronic Systems, Warsaw University of Technology, [2]GSI - Helmholtzzentrum für Schwerionenforschung GmbH

Introduction

The CBM experiment in Darmstadt is being prepared. The production of components for the readout chain is ongoing.
The key element for the readout of STS and MUCH detectors is the dedicated STS-MUCH-XYTER 2.2 (in short, SMX) ASIC developed by AGH in Kraków [1].
The SMX ASICs are mounted on front-end boards (FEBs) in various configurations depending on the detector system and expected hit rates.
The readout is done with GBTX-based [2] CROB boards further connected to the CRI data concentration backend.



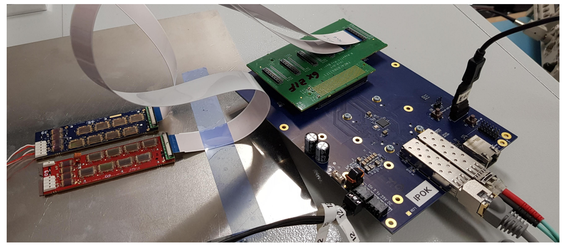
Simplified block diagram of the SMX-based CBM readout chain

Assembled STS Detector module in its test setup

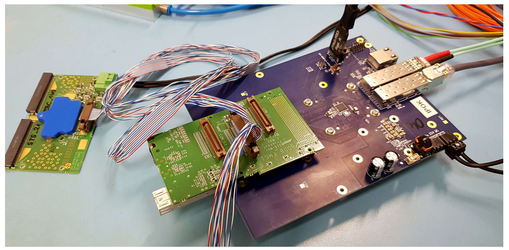
FEB8 boards

Motivation for tester development

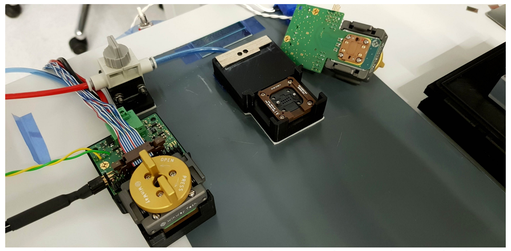
Testing produced ASICs, assembled FEBs, and full modules is the essential quality verification step in the production process.
Neither the tester prepared during the development of the SMX and communication protocol [3] nor a limited subset of the CBM readout chain can be used for testing due to the high cost of components or their limited availability (the GBTX chip is subject to export restrictions).
The GBTxEMU board was developed as a cheap and widely available replacement for GBTX-based CROBs [4]. It provides broad availability of tester hardware for production in various sites and additionally allows full system tests in collaborating institutions worldwide independently of the GBTx-based readout. It can be used either as an emulator of the GBTx data readout board alone or as a full standalone backend system for FEB control.



Tester with the FMC board enabling connection of FEB8 boards. Two such boards are connected.



Tester with the FMC board enabling connection of FEB-C boards or pogo-pin tester. One FEB-C board visible.



The pogo-pin tester used for testing unbounded, bare SMX chips.

GBTxEMU-based tester

The GBTxEMU board is based on a standard commercial Artix-7 board (TE-0712, Trenz Electronics GmbH).
The board is supplemented with a dedicated motherboard providing necessary connectors, communication interfaces, and a jitter cleaning device (SiLabs Si5344).
It allows for clock recovery and system-wide synchronization if used in GBTx emulating mode.
The tester IP cores have been developed for this Artix-7 platform, based on the GBTxEMU board and the developments for the new CRI-based readout in CBM.
The tester supports communication with the SMX ASICs on various FEBs, employing various numbers of connected ASICs and readout E-Links, interfaced with different VITA 57.1 FMC adapters.

E-Link emulation

GBTxEMU emulates E-Links with phase adjustable clocks otherwise provided by the GBTx ASICs with a clock frequency set to 40, 80, or 160 MHz. The clock phase may be adjusted with a resolution offered by the MMCM blocks (1/1600 MHz/8 = 78 ps, slightly worse than 48.8 ps offered by GBTx). The input data delay may be adjusted with the IDELAYE2 blocks providing the resolution of 78 ps with a 200 MHz reference clock.

The tester software

The tester is controlled via the IPbus interface over 1 Gb/s Ethernet. With the accompanying software written in Python, the tester supports full testing of the E-Link communication. It also provides access to all internal registers of the SMX chips, enabling complete functional tests.
The received ASIC hit data may be stored in an internal FIFO accessible via IPbus, enabling the direct collection of a limited amount of hit data at a high hit rate. For longer tests at a limited hit rate, the possibility to transmit the hit data from selected channels in UDP packets has been implemented.

Tester in the GBTX-emulation mode

The tester is hardware-compatible with the GBTxEMU firmware. That allows the sites equipped with the prototype versions of the CBM readout chain to connect the tester via an emulated GBT optical link and perform long-time tests at a high rate.

Conclusions

The tester is a versatile tool enabling testing of the SMX ASICs at the manufacturing site and the mounted FEBs and assembled detector modules - both after manufacturing and after delivery, before mounting in the detector. The FPGA-based design offers high flexibility. The Python-based software also may be easily modified and adapted to the user's particular needs, including interfacing with the higher-level operation and quality verification software.

References

[1] K.Kasinski et al., "STS-XYTER, a high count-rate self-triggering silicon strip detector readout IC for high resolution time and energy measurements", doi:10.1109/NSSMIC.2014.7431048
[2] P.Leitao et al., "Test bench development for the radiation Hard GBTX ASIC", doi:10.1088/1748-0221/10/01/C01038
[3] W.M. Zabołotny et al.,"Design of versatile ASIC and protocol tester for CBM readout system", doi: 10.1088/1748-0221/12/02/C02060
[4] W.M.Zabolotny et al., “GBTx emulation for BM@N/MPD data acquisition systems”, doi:10.5506/APhysPolBSupp.14.555

Acknowledgements

The work has been partially supported by GSI, and partially by the statutory funds of Institute of Electronic Systems.