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SMX and front-end board tester for CBM readout chain

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The SMX chip is a front-end ASIC dedicated for the readout of STS and MUCH detectors in the CBM experiment.
The production of the ASIC and the front-end boards based on it is just being started and requires thorough testing to assure the quality.
The paper describes the SMX tester based on a standard commercial Artix-7 FPGA module with an additional simple baseboard.
In the standalone configuration the tester is controlled via IPbus and enables full functional testing of connected SMX, FEB, or a full detector module.
The software written in Python may easily be integrated with higher-level testing software.

Summary (500 words)

The production of components for the readout chain of the CBM experiment is ongoing.
The readout of the STS and MUCH detectors in CBM uses the dedicated STS-MUCH-XYTER 2.2 (in short, SMX) developed by AGH Krakow.
The SMX ASICs are mounted on front-end boards (FEBs) in various configurations depending on detector system and expected hit rates.
Readout is done with GBTx-based CROB boards further connected to CRI data concentration backend.
Testing of produced ASICs, assembled FEBs and full modules is the essential quality verification step in the production process.
The GBTxEMU board has been proposed as a common platform for all testing setups with two benefits: It provides broad availability of tester hardware for production in various sites and additionally allows full system tests in collaborating institutions worldwide independently of the GBTx-based readout.
It can be used either as an emulator of the GBTx data readout board alone or as full standalone backend system for FEB control. The GBTxEMU board is based on a standard commercial Artix-7 board (TE-0712, Trenz Electronics GmbH).
The board is supplemented with a dedicated motherboard providing necessary connectors and communication interfaces and a jitter cleaning device (SiLabs Si5344). It allows for clock recovery and system-wide synchronization if used in GBTx emulating mode.
The tester IP cores have been developed for this Artix-7 platform, based on the GBTxEMU board, and the developments done for the new CRI-based readout in CBM.
The tester supports communication with the SMX ASICs on various FEBs, employing various numbers of connected ASICs and readout E-Links, interfaced with different VITA 57.1 FMC adapters.
It emulates E-Links with phase adjustable clocks otherwise provided by the GBTx ASICs with a clock frequency set to 40, 80, or 160 MHz. The clock phase may be adjusted with a resolution offered by the MMCM blocks (1/1600 MHz/8 = 78 ps, slightly worse than 48.8 ps offered by GBTx). The input data delay may be adjusted with the IDELAYE2 blocks offering the resolution of 78 ps with a 200 MHz reference clock.
The tester is controlled via the IPbus interface over 1 Gb/s Ethernet. With the accompanying software written in Python the tester supports full testing of the E-Link communication. It also provides access to all internal registers of the SMX chips, enabling complete functional tests.
The received ASIC hit data may be stored in an internal FIFO accessible via IPbus, enabling the direct collection of a limited amount of hit data at a high hit rate. For longer tests at a limited hit rate, a possibility to transmit the hit data from selected channels in UDP packets has been implemented.
The tester is hardware-compatible with the GBTxEMU firmware. That allows the sites equipped with the prototype versions of the CBM readout chain to connect the tester via an emulated GBT optical link and perform long-time tests at a high rate. The Python-based software may be easily modified and adapted to the user's particular needs, including interfacing with the higher-level operation and quality verification software.

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