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Single Event Effects on the RD53B Pixel Chip Digital Logic and On-chip CDR

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The RD53B chip for HL-LHC upgrades of ATLAS and CMS needs to provide reliable operation in a radiation hostile environment with inevitable Single Event Effects. To answer the challenge, substantial efforts are made to protect and evaluate the critical parts of digital logic with different TMR schemes and to characterize the on-chip CDR. Cross-section for each TMR scheme and its effective SEE sensitivity are measured in several SEE campaigns. The on-chip CDR is characterized by measuring the SEE-induced phase shifts of its output clocks and their implication on the high-speed link stability. Results from these campaigns will be presented.

Summary (500 words)

The RD53B chip is designed with the goal of having a high tolerance for Single Event Effects (SEE). In order to gain an increased immunity for SEEs, critical parts of the digital logic such as chip configuration registers and pixel configuration bits are designed with TMR protection. As a trade-off between area, power consumption and SEE immunity, global configuration registers are protected by TMR protection with auto-correction, while pixel configuration registers lack the auto-correction in their TMR protection scheme.

Measured cross-sections in two SEE campaigns at CRC, Louvain la Neuve, show that adding a triplication scheme with a voter and with no auto-correction to the single latch will decrease its effective SEE sensitivity one to two orders of magnitude, depending on the ion LET. By adding auto-correction to this protection scheme, one more order of magnitude decrease is achieved. The measurements with a 480 MeV proton beam in TRIUMF, Canada, showed that gain achieved with no auto-correction inside TMR scheme is 100, and adding auto-correction will increase this gain to 400. During these campaigns, it has been observed that the 1.28Gbit/s link can lose its synchronization which has led to lost or corrupted data events. However, this behavior was not seen when the required clocks are provided externally by bypassing the on-chip CDR. Motivated by this, a dedicated CDR testing campaign was done in GANIL, France. The goal was to characterize SEE-induced phase shifts in the CDR clocks and their implications on the corrupted data events and overall high-speed link stability. For such a test, two setups were used in parallel. The first one was an oscilloscope triggered on the serializer clock phase shift larger than 400ps in respect to the stable clock reference. The second setup was based on a 10.24Gbit/s clock oversampler inside the FPGA, reaching the resolution of 97ps. All SEE-induced events captured by these 2 setups can be classified into several categories, depending on the behavior of the clock's phase, frequency, biasing, and amplitude. The different nature of captured events points to different chip parts being sensitive to SEEs, such as different blocks of the CDR itself, the LVDS receiver, and the CML driver.

These results, conclusions and setup descriptions are relevant for radiation tolerant systems, general testing and system reliability, as well as an important step in preparing for a stable operation of detectors in HL-LHC.

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