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Fully-integrated set-up for gate current characterization in 28nm CMOS technology

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This work introduces design and simulation validation, of a monolithic setup, based on a current amplifier, for accurate gate current measurement in NMOS devices integrated in 28nm technology. The Devices-Under-Test (DUTs) include transistors with gate width between 60µm and 300µm and length between 400nm and 1µm. Current in the DUT is amplified by a 100x factor, with an accuracy above 90%. The current amplifier achieves low noise operation for an accurate gate-current parallel noise estimation. The device will also be exploited to study radiation (up to 500Mrad-TID) damage effects on the noise current and on its associated parallel noise.

Summary (500 words)

The requirement for increased IC components density in read-out systems for High Energy Physics (HEP) experiments led, in the last decade, and will lead, in the future upgrades, to an extensive exploitation of deep-submicron technologies (65nm and below). These highly downscaled nodes suffer from a reduction in the gate oxide layer thickness (nowadays less than 2nm), which can be strictly correlated with an increased gate-channel direct tunneling phenomena. This situation translates in an increase in the MOSFET Gate Current (IGate), resulting in digital power consumption increase and analog device noise performance worsening. To Study the relationship between the gate current and the most important transistor design parameters, the impact of this current on analog performances, and the effect of radiation on the current value itself, has become of crucial importance.

Within the INFN project FinFet16v2, this work proposes a gate current amplifier in 28nm CMOS technology achieving a 40dB current amplification. This large amplification is a mandatory requirement for measuring such small currents, in the nA range, and distinguish it from the noise floor. To achieve the desired task, the circuit represented by the schematic of fig.1 has been developed. The DUT gate current is sensed by M21 and mirrored in M22 with a mirror factor of 9. M7 provides both transistors with their bias current, which will be mirrored in a 10-times wider M23 transistor, yielding an output current a factor of 100 larger than the original gate current.

More than 90% accuracy in the ratio between the output current and the gate current in the Device-Under-Test (DUT) is achieved thanks to proper design and layout precautions. Transistor M30 is designed to match M22 and M21 and provides M7 and M23 with the same bias conditions. The most important transistor couples (M23-M7 and M22/M21-M30) are laid out in an interdigitated fashion to maximize device matching and improve accuracy, in corner and Montecarlo simulations. A capacitive feedback path (C1) was implemented for stability purpose.

The same gate current amplifier can be operated with DUT featuring different gate size, with width between 60µm and 300µm and length between 400nm and 1µm, making it possible to characterize the gate current as a function of the transistor size. In this prototype setup overall 20 different DUTs are available. Moreover, since gate current also depends on the transistor bias point, the drain-source current in the DUT can be tuned, by properly trimming the Ibias_tuning between 100µA and 5mA. In simulation, the measurable gate current with these setup conditions ranges between 0.3nA and 157nA.

Last, thanks to the proper feedback loop and an accurate transistor sizing, the DUT gate current noise can be assumed as the dominant contribution in the overall current noise at the amplifier output. For this reason, the gate current amplifier can be exploited for accurate gate current noise measurement.

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