Successive Approximation Register ADC
Single Event Effects Protection and Evaluation

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Introduction

Analog-to-digital converters (ADCs) are critical parts of numerous acquisition systems in HEP experiments. There are several possible architectures to design an ADC and a popular one is the successive approximation register (SAR). This work analyses seven different alternatives to implement an ADC based on the SAR architecture in relation to protection strategies against single event upsets, including the comparison of per module and per cell triplication, its reset and encoding.

ADC Architecture

The SAR ADC is a mixed-signal block and may be implemented using a comparator, a DAC and a control module. The last one is a digital block named SAR which is responsible to run the successive approximation algorithm, triggering the sampling, controlling the DAC switches and reading the comparator responses. This digital block can suffer from single-event effects (SEE) generated by interactions with radiation, causing inappropriate control of the other blocks and creating incorrect conversions.

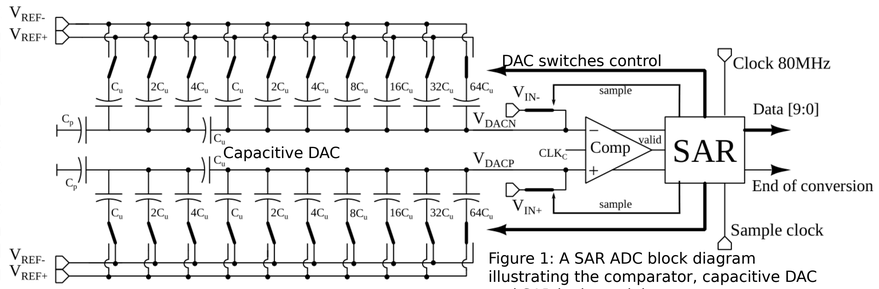

Figure 1: A SAR ADC block diagram illustrating the comparator, capacitive DAC and SAR logic module.

Designed Prototypes

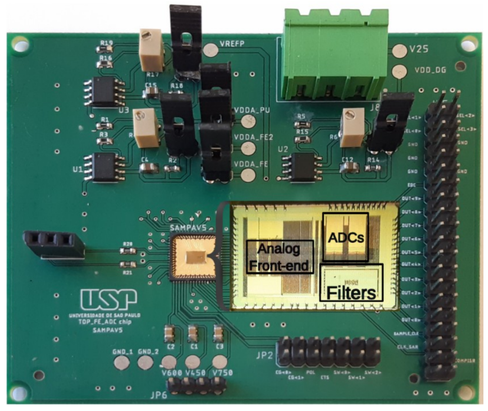

Figure 2: Test board with the open package and a zoomed version of the die showing its internal blocks.

Nine blocks were designed in TSMC 130nm technology, where two encoding options were compared, binary and one-hot. Two reset/sampling control options were also tested, the synchronous and asynchronous forms. In relation to protection to SEE, three versions were done, one unprotected, one with per register TMR and one with three complete blocks with voting between them (Modular TMR). Three reference ADCs were also inserted and identified as ADC0, ADC1 and one with parity at the output PADs (ADC0P).

Block ID	Name	Encoding	Protection	Reset
ADC0	ADC	one hot	none	asynchronous
ADC1	ADC	one hot	none	asynchronous
ADC0P	ADC + Parity	one hot	none	asynchronous
sar_reg_03	sar_reg5_notmr_hot	one hot	none	synchronous
sar_reg_04	sar_reg5_tmr_hot	one hot	TMR	synchronous
sar_reg_05	sar_reg5_mod_hot	one hot	Modular TMR	synchronous
sar_reg_06	sar_reg5_notmr_bin	binary	none	synchronous
sar_reg_07	sar_reg5_tmr_bin	binary	TMR	synchronous
sar_reg_08	sar_reg5_mod_bin	binary	Modular TMR	synchronous

Irradiation Campaign

The blocks were packaged in an open-window QFN64 which was soldered to a minimal board just with supply components and tested using a Sockit FPGA which was placed outside of the irradiation chamber.
The open package allowed direct access to the die and the irradiation chamber was kept in vacuum to minimize the beam losses.
The ASIC was irradiated using the Pelletron particle accelerator at the IFUSP (Physics Institute of São Paulo University). Three different beam types were used, starting with 5 MeV alpha particles and going to 44 MeV $^{16}O^{7+}$ and finally 57 MeV $^{28}Si^{8+}$.

Particle	Energy [MeV]	LET $[MeV/(mg/cm^2)]$
α	5	0.65
^{16}O	44	6.4
^{28}Si	57	13.6

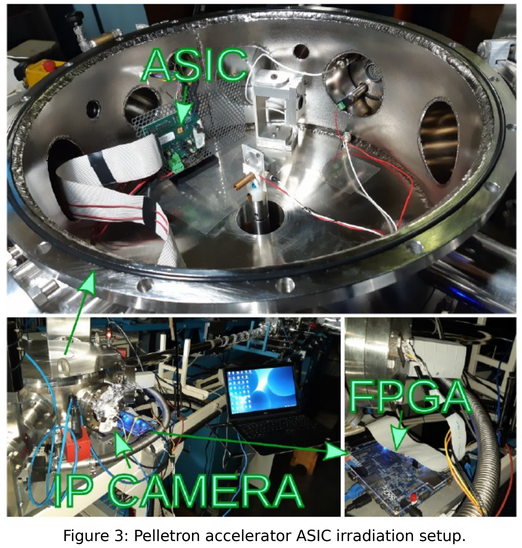

Figure 3: Pelletron accelerator ASIC irradiation setup.

Results

The blocks were irradiated in 8 main test runs divided between the reference unprotected ADCs (ADC0, ADC1, ADC0P) and the proposed ones (sar_reg_03 to sar_reg_08). The results for the reference ADCs were grouped as a single entry named ADC in the result tables.
No major destructive failures happened and the analysis focused on the SEUs (Single Event Upsets) and SETs (Single Event Transients) triggered errors.
The output errors were accounted by the FPGA and the cross-sections computed.
The MTBFs (Mean Time Between Failures) presented are the expected for a particle flux of $3.4{\cdot}10^3$ /cm² s.
It is important to note that SETs in the path between the chip and FPGA were extremely rare and can be ignored, as measured by the parity.
The cross-sections measured shown that using asynchronous reset/sampling can cause major sensibility to SEE greatly reducing the MTBFs due to interrupted conversions and corrupted results.
The coding of the FSM and interface to the DAC control switches also impacted the cross-sections, where using one register per bit (one-hot) was worse than binary coding it, and expanding this with combinatory logic. One-hot increased the cross-section by more than 37%.
The redundancy with replication was enough to keep the block free of error for all the cases. The full block triplication behaved similarly than the triple registers with voters, but register replication allowed a cell area reduction of 34%.

Block ID (Name)	Cell Count	Cell Area $[\mu m^2]$	Final Area $[\mu m^2]$	Design Density	MTBF [s]
ADC	94	1845	7432.56	24.82%	< 20
sar_reg_03 (notmr_hot)	116	1673	7345.28	22.78%	< 565
sar_reg_04 (tmr_hot)	272	4375	7345.28	59.56%	> 28000
sar_reg_05 (mod_hot)	416	5935	7345.28	80.80%	> 28000
sar_reg_06 (notmr_bin)	114	1561	7345.28	21.25%	< 766
sar_reg_07 (tmr_bin)	249	3691	7345.28	50.25%	> 28000
sar_reg_08 (mod_bin)	413	5581	7345.28	75.98%	> 28000

Block ID	Ion Name	Run Name	Flux $[10^3/(cm^2 s)]$	Fluence $[10^6/cm^2]$	Event Count	Cross-section $[cm^2]$
ADC	^{16}O	t8	819.0	368.2	5932	$(1.60 \pm 0.03){\cdot}10^{-5}$
sar_reg_03	^{16}O	t7	918.5	291.9	140	$(4.80 \pm 0.41){\cdot}10^{-7}$
sar_reg_04	^{16}O	t7	918.5	291.9	0	$< 1.02{\cdot}10^{-8}$
sar_reg_05	^{16}O	t7	918.5	291.9	0	$< 1.02{\cdot}10^{-8}$
sar_reg_06	^{16}O	t7	918.5	291.9	102	$(3.49 \pm 0.35){\cdot}10^{-7}$
sar_reg_07	^{16}O	t7	918.5	291.9	0	$< 1.02{\cdot}10^{-8}$
sar_reg_08	^{16}O	t7	918.5	291.9	0	$< 1.02{\cdot}10^{-8}$

Conclusions

An ASIC containing several implementations of a 10-bit SAR was designed, produced and packaged.

The device was irradiated in a campaign on the Peletron particle accelerator at the University of São Paulo using alpha particles, ^{16}O and ^{28}Si.

The reset strategy and conversion start signals were found to be very important to the block sensitivity to single events and the amount of asynchronous logic should be minimized.

The encoding used in the SAR state machine was evaluated and it also impacts the cross-section of the device, being the ADC standard one-hot approach more sensitive than the simple binary encoding, which represents an improvement of about 27%.

The use of triplication was essential to achieve day-long MTBFs and no sensitive difference was measured between the per register and per module strategies within the tested ranges.

With protection, the SAR achieved MTBF improvements of more than 4200 times.

Acknowledgement

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