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Successive Approximation Register ADC Single Event Effects Protection and Evaluation

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This work analyses seven different alternatives to implement an ADC based on the successive approximation register (SAR) architecture. The influence of the encoding is taken into account while evaluating the importance of its reset approach. Different protection strategies against single event upsets are addressed, including the comparison of per module and per cell triplication. All versions of the SAR were designed and prototyped in the TSMC 130 nm technology. The ASIC was packaged in an open window QFN64 and irradiated in the IFUSP Pelletron particle accelerator, which revealed the impact of the encoding and reset choices in the block cross-section.

Summary (500 words)

ADCs are critical parts of numerous acquisition systems in HEP experiments. There are several possible architectures to implement an ADC and a popular one is the successive approximation register (SAR).

The SAR ADC is a mixed-signal block and may be implemented using a comparator, a DAC and a control module. The last is a digital block named SAR register which is responsible to run the successive approximation algorithm, triggering the sampling, controlling the DAC switches and reading the comparator responses. Moreover, it is responsible to register the calculated conversion and send it to further digital processing steps.

This digital block can suffer from single-event effects (SEE) generated by interactions with radiation, causing inappropriate control of the other blocks and creating incorrect conversions. Another possibility is the occurrence of single-event upsets (SEU) in a completed conversion value. These events can corrupt experiment data and should be investigated and mitigated.

To accomplish that, seven implementations of a 10 bit SAR were designed using different approaches in its digital control, but still focusing on not changing its analog side, triplicating it, or doing extra conversions.

Table 1 shows the implemented alternatives where two encoding options were done, binary and one-hot, also two reset options were tested synchronous and asynchronous. In relation to resistance to SEE three versions were done, one unprotected, one with per register TMR (Triple Modular Redundancy) and one with three complete blocks with voting between them (identified as Modular TMR). Three reference versions were also inserted and identified as ADC0, ADC1 and ADC0 with parity at the output.

The blocks were fabricated in TSMC 130nm process and packaged in an open-window QFN64 which was soldered to a minimal board just with supply components and tested using a Sockit FPGA which was placed outside of the beam chamber. Figure 1 illustrates the board together with the chip microphotography and Figure 2 shows the test scenario.

The ASIC was irradiated using the Pelletron particle accelerator at the São Paulo University. Three different beam types were used, starting with 5 MeV alpha particles and going to 44 MeV ^{16}O and finally 57 MeV ^{28}Si. Due to the low event count, the alpha particle test was discarded.

Table 2 provides the compiled cross-section results. Comparing the reference with sar_reg_03, a 70 times bigger cross-section is found, where the major difference is the asynchronous reset, showing that it increases the sensitivity and may be avoided.

In relation to the coding, a worse performance (greater than 140%) happened when using the one-hot in the state machines.

No considerable difference was found when changing the redundancy to the bigger modular strategy and both TMR alternatives have been successful.

Finally, is possible to state that there are positive results in relation to the evaluation of the inserted protections since, for all cases with some level of redundancy, no errors were registered. And this scenario was repeated for all the bundles and all the flows illustrating a great improvement in relation to the reference in this aspect.

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