# Readiness of the radiation tolerant link Daughterboard for the High Luminosity upgrade of the ATLAS Tile Calorimeter

## (1) The **ATLAS** Hadronic **Tile Calorimeter (TileCal).**

TileCal ATLAS hadronic sampling calorimeter[1]. The detector is composed of plastic scintillator tiles as active material interleaved with steel plates as absorber. The detector is divided in four cylindrical barrels composed of 64 wedge-shaped modules each (Fig. 1). The scintillators in each module are grouped in pseudo-projective cells. Light from two sides of a cell is collected by wavelength shifting fibers and read out by two photomultiplier tubes (PMTs). The High Luminority Large Hadron Collider (HL-LHC) will have an instantaneous luminosity of 5 times the LHC nominal design value. The ATLAS TileCal read-out electronics will be incapable of dealing with the with the higher radiation levels and increased rates of pileup. R&D is ongoing aimed to replace a TileCal electronics with a improved design that will provide continuous digital read-out of all TileCal with better timing, better energy resolution and less sensitivity to out-of-time pileup [1].

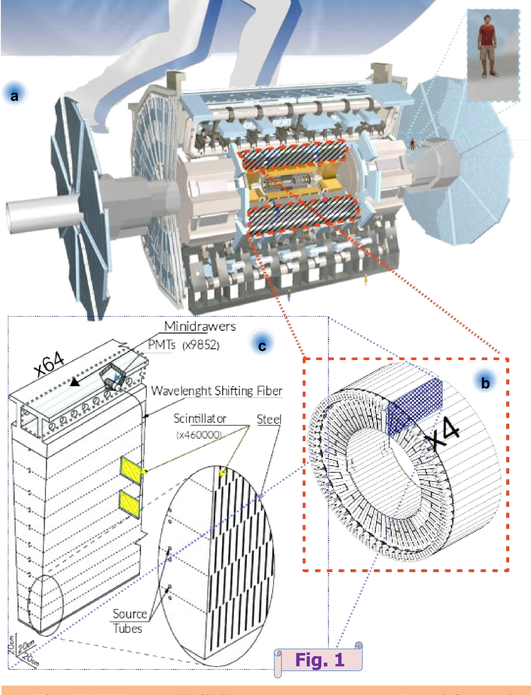

Fig. 1

## (3) The **Daughterboard revision 6.**

The **DB** is a redundant radiation tolerant board that serves as the read-out link and control hub between on- and off-detector electronics by means of a **400-pin FMC** connector and **four SFP+** respectively. The design is divided in two functionally-equal halves that receives commands and clocks recovered by the **CERN rad-hard GBTx** through a **4.8 Gbps GBT-FEC downlink**. On each half of the DB, A 20 nm planar **Xilinx Kintex Ultrascale (KU) FPGA** distributes the clocks and configuration received from the GBTx to the MB, reads-out digitized data from two different gains of each of six PMT channels of the MD and reads out digitized data from six channels of a slow charge integrator ADC. Additionally, the xADC of each KU FPGAs samples temperature, voltage stability, currents, and additional digitized data from the xADC interface. Each KU FPGA sends data off- detector by means of two copies of GBT-CRC protected words through two 9.6 Gbps uplinks. The board radiation tolerance is achieved by the **redundancy layers** in the design, using the **Xilinx Soft Error Management (SEM)** and **Triple Mode Redundancy (TMR)** wherever allowed in the firmware and using **GBTx** and **GBT-FEC** protocol

Compared to its predecessors, the **DB revision 6 (DB6,** Fig. 4**)**:

- **Improves the firmware clocking and timing scheme** by taking advantage of the Ultrascale dedicated XYPHY BITSLICE byte architecture for the ADC read-out, and routing the diverse clock network using GC buffers to distribute the clock signals within the different banks to allow better timing closure and minimal routing congestion during the firmware implementation [5] (Fig. 7).
- **Minimizes single points of failure** by using 130 nm flash based **Lattice ICE40 FPGAs** to buffer and control start-up and remote resets of GBTxs and KU FPGAs, and the JTAG interfaces of the KU FPGAs and attached FLASH memories, mitigating any downlink failures causing signals being propagated from the GBTx Eports .
- **Increases the radiation tolerance** by using **20 nm TSMC planar technology Ultrascale FPGA** that is not sensitive to **Single event Latchups (SEL)** as the **16 nm FinFET Kintex Ultrascale+ (KU+)** and has less **Single Event Upsets (SEUs)** than the **28 nm plannar Kintex 7 (K7)**[2][3], and re-design of the power-on sequence to a chain of DC-DC converters integrated with an **SEL current limiting circuitry** that will increment the robustness of the board on the presence of isolated overcurrents.

## (2) The **HL-LHC** read-out system.

The **off-detector electronics** (Fig. 3) will provide digitized signals at 40 MHz to the **Level 0 (L0)** trigger system through the **Trigger and DAQ interface (TDAQi),** and the the **FELIX** system will read-out data stored in pipelines in **Tile Preprocessors (TilePPr)** at 1 MHz. The **TilePPrs** will interface the on- and off-detector electronics through multi-GBps optical links

The power will be monitored and distributed to the on-detector electronics by:

- **Detector Control System (DCS)** to interface with the **Low Voltage Power Supply (LVPS)**
- **High Voltage Power Supply (HVPS)** to provide high voltage to each **PMT**

The **on-detector electronics** will continuously sample data from all TileCal PMTs at **40 MHz** (Fig. 3) by means of **896 Minidrawers (MDs,** Fig. 3**)**. A **MD** will host up to **12 channels** by means of:

- **a Daughterboard (DB,** Fig. 4**)** to distribute **LHC synchronized timing**, configuration and control to the front-end, and **continuous read-out** of the digital data from all the MB channels to the off-detector systems via multi-Gbps optical links,
- **a Mainboard (MB)** to continuously sample and digitize **two gains** of shaped PMT signals,
- **12 Front-End Boards (FEBs)** to shape and condition the PMT signals,
- **12 PMTs** to turn light pulses to electric signals.

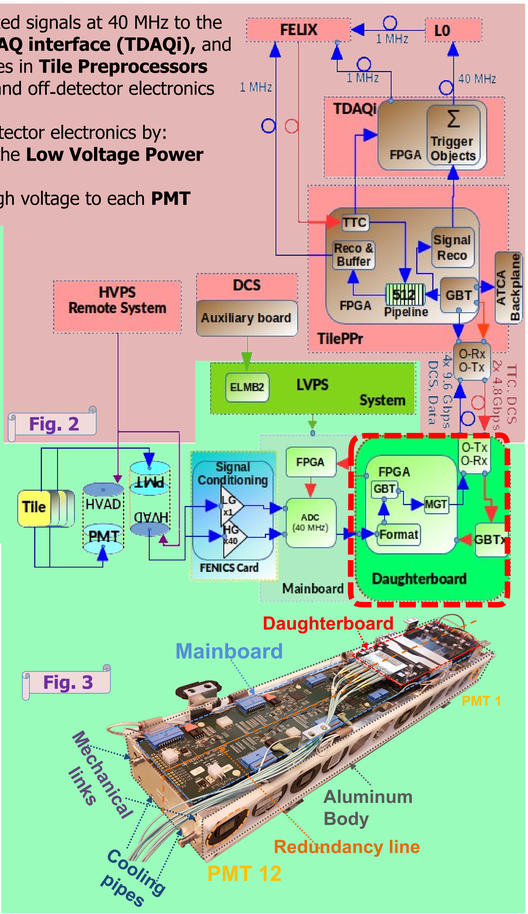

Fig. 3

## (4) **Radiation tests** results.

- To test for **Total Ionizing Dose (TID)** two DB6s (DB6_1 and DB6_2) were irradiated with a $Co^{60}$ at the CERN CC60 facilities with different dose rates and different dose targets. DB6_1 was irradiated to 220 Gy at a "fast" rate of 3.37 Gy/h and DB6_2 was irradiated to 52.6 Gy at a "slow" rate of 0.33 Gy/h.
- The KU FPGAs and all the currents were monitored for each of the voltages of each half of the two boards (Fig. 5), putting special interest in the eight Coretek SFP+, the four KU FPGAs, the four Microsemi ProaSIC3 FPGAs and the reconfiguration FLASH memories. None of the components were damaged by the TID.
- In the case of DB6_1 (Fig 5. a, Fig 5. b), strong correlations between temperature and current in 0.95 V were demonstrated. An increase in current was measured in the 0.95 V of both sides at around 140 Gy strongly seems to be correlated with the failure of the active components of the fan used to keep the KU FPGAs cool leading to the increase of temperature on the FPGA. In the case of DB6_2 (Fig. 5 c, Fig 5. d), all the currents and the temperatures were stable during the full run.

- To test for Single Event Effects **(SEE)** two Trenz TE0841 boards (each with the same KU FPGA used in the DB design), a Lattice ICE40LP FPGA and a ProASIC3E A3P31500 FPGA were irradiated with 226 MeV protons to achieve a target fluence of 1.11E+12 p/cm2, eight times the fluence simulated for 10-years of HL-LHC.
- During the test, all the currents of the FPGAs were monitored (Fig. 6) and no sign of **Single Event Latchups (SEL)** was detected.
- The LCMXO2 CPLDs of the TE0841 boards in control of buffering the JTAG chains for configuring the KU FPGAs failed due to TID effects. Consequently, only rough estimates of the **Single Event Upsets (SEUs)** could be obtained through the **Xilinx SEM** over two runs: 2 uncorrectable errors and 2333 correctable errors for a rate of ~166 soft errors per 10E9 p/cm2.
- The firmware of the ProASIC3E A3P31500 started failing at around 75% of the total fluence (~570 Gy of TID). The firmware functionality was recovered after a process of annealing. However, the VPUMP of the FPGA was permanently damaged so reconfiguration of the chip is not possible (in agreement [6])
- The Lattice ICE40LP FPGA firmware failed after ~1E10 p/cm2 of the delivered fluence. The firmware functionality was recovered on-site by reconfiguring the FPGA from the attached PROM after power-cycle.
- **Non-Ionizing Radiation Losses (NIEL)** will take place in a neutron reactor during the end of 2021.

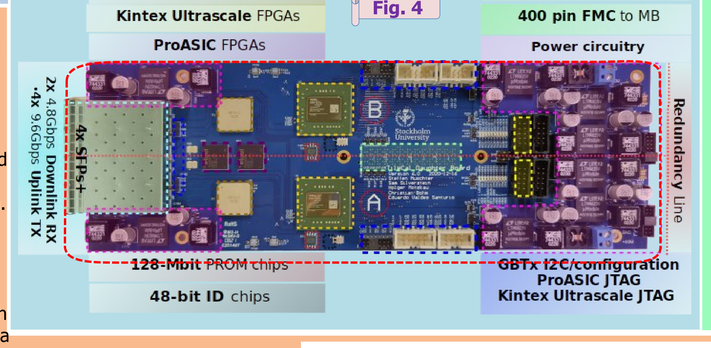

Fig. 4

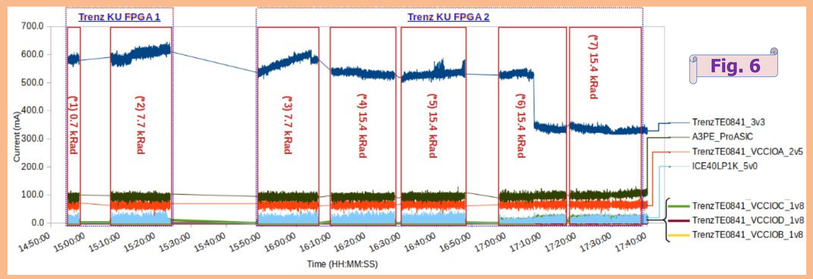

Fig. 6

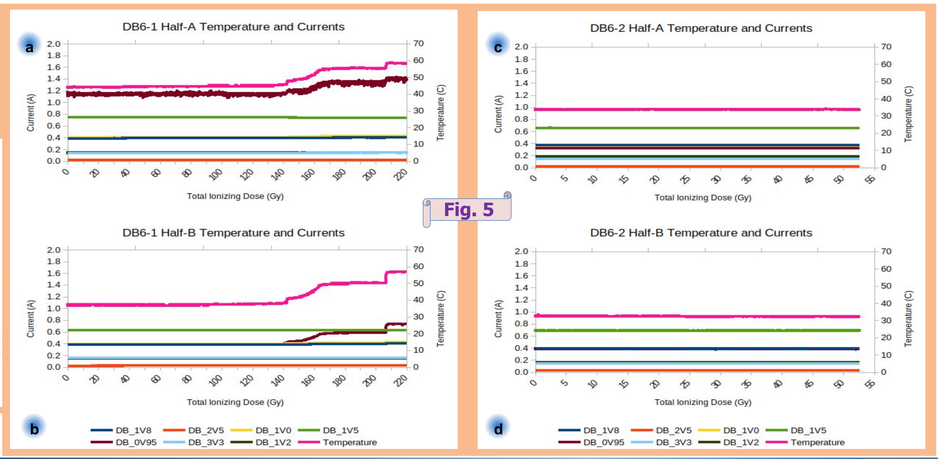

Fig. 5

## (5) Relevant references.


[1] ATLAS collaboration. Technical Design Report for the Phase-II Upgrade of the ATLAS Tile Calorimeter. CERN-LHCC. 234 2017-019, ATLAS-TDR-028, 2018
[2] ATLAS Tile Calorimeter Link Daughterboard, PoS Volume 343 - Topical Workshop on Electronics for Particle Physics (TWEPP2018), DOI: 10.22323/1.343.0024
[3] Single Event Upset Characterization of the Zynq UltraScale+ MPSoC Using Proton Irradiation, 2017 IEEE Radiation Effects Data Workshop (REDW), DOI: 238 10.1109/NSREC.2017.8115448
[4] Single-Event Latch-Up: Increased Sensitivity From Planar to FinFET, 2017 IEEE Radiation, IEEE Transactions on Nuclear Science 2018, DOI: 10.1109/TNS.2017.2779831
[5] A revised version of the ATLAS Tile Calorimeter link Daughterboard for the HL-LHC.IEEE Transactions on Nuclear Science 10.1109/TNS.2021.3103408
[6] Radiation_tolerant_proasic3_fpgas_radiation_effects_report (131374). https://www.microsemi.com/document-portal/doc_view/131374-radiation_tolerant_proasic3_fpgas_radiation_effects_report


## (6) Conclusions.

The DB6 fulfills the HL-LHC radiation requirements for TID and SEEs. The DB6 uses the KU architecture that has higher SEU rates than DB5 (KU+ FPGA) and less SEU rates than the DB4 (K7), the sensitivity to SEL present on the KU+ FPGAs is unacceptable for ATLAS on-detector electronics. The DB6 was successfully tested for TID and SEE, and will be tested for NIEL in the end of 2021. The performance DB6 is being tested with the upgrade system in a testbeam. A Preliminary Design review will take place during December 2021. Around 930 DB6 will be produced as the contribution of Stockholm University to the HL-LHC era for TileCal.


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