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Readiness of the radiation tolerant link Daughterboard for the High Luminosity upgrade of the ATLAS Hadronic Calorimeter

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The upgrade of the ATLAS TileCal for the HL-LHC uses a Daughterboard that serves as a hub interfacing the on-detector with the off-detector electronics. The Daughterboard design features ProASIC FPGAs, Kintex Ultrascale FPGAs and CERN GBTx ASICs. The design minimizes single points of failure and radiation damage by employing a double-redundant scheme, using TMR and Xilinx SEM strategies, adopting CRC verification in the uplinks and FEC in the downlinks, and using a dedicated SEL protection circuitry. We present a summary of the studies on the Daughterboard revision 6 performance and the radiation qualification tests of the design components.

Summary (500 words)

The upgrade of the ATLAS Hadronic Calorimeter for the High Luminosity Large Hadron Collider (HL-LHC) has motivated progressive redesigns of a radiation tolerant link Daughterboard that serves as a hub interfacing the on-detector with the off-detector electronics via two 4.6 Gbps downlinks and two pairs of 9.6 Gbps uplinks powered by four SFP+ Optic transceivers. Configuration commands and LHC timing are received by the downlinks to be propagated to the front-end through two Microsemi ProASIC FPGAs, two CERN radiation hard GBTx ASICs and two Kintex Ultrascale FPGAs. In parallel, the Kintex FPGAs send continuous high-speed readout of digitized PMT samples, detector control system and monitoring data through the uplinks. The Daughterboard design minimizes single points of failure and radiation damage by employing a double-redundant scheme, using Triple Mode Redundancy (TMR) and Xilinx Soft Error Mitigation (SEM) in the FPGAs to mitigate Single Event Upset (SEU) rates, adopting Cyclic Redundancy Check (CRC) error verification in the uplinks and Forward Error Correction (FEC) in the downlinks, and using a dedicated Single Event Latchup (SEL) and over-current protection circuitry to avoid hardware damages.

Around 930 Daughterboards will be produced as the contribution of Stockholm University to the the ATLAS Upgrade for the HL-LHC era. Before settling on a final board design that could be taken into a production stage, radiation test campaigns have taken place to qualify the different components of the board for Total Ionizing Dose (TID), Non Ionizing Energy Losses (NIEL) and Single Event Effects (SEE). The Kintex Ultrascale FPGA firmware has a complex clock distribution and a timing scheme with multiple clock inputs, some of them to be multiplexed accordingly to the firmware needs. The clock inputs come from various sources such as the two GBTxs, an oscillator and the six ADCs sitting on a MB side. The PCB design and the firmware was optimized so that the Kintex ultrascale FPGA can manage more than 18 independent clock inputs to drive all the required functionalities. Besides testing the clocking scheme, the set of tests performed to verify the DB core functionalities include GTH link reliability and stability tests, IDDR-SERDES readout reliability and stability tests, GBTx-ConfigBus configuration bus interface, current and power monitoring system.

We present a summary of the studies that took place to verify the reliability if the Daughterboard revision 6 design performance, and the radiation qualification tests of the components used for the design.

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