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Readout electronics for the CMS Phase II Endcap Calorimeter: system overview and prototyping experience

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The frontend readout system for the silicon section of the CMS Phase II Endcap Calorimeter faces unique challenges due to the high channel count and associated bandwidth, limited physical space, as well as radiation tolerance requirements. This presentation will give an overview of the frontend electronics design and will discuss the recent experience obtained from the first test system that integrates the HGCROC2 readout ASIC, lpGBT, and VTRX+ in a realistic manner, linking together prototypes of the hexaboard, engine board, and wagon board.

Summary (500 words)

The CMS endcap calorimeters will be fully replaced as part of the Phase II upgrade. The upgraded detector (known as HGCAL) will be a sampling calorimeter featuring integrated electromagnetic and hadronic sections, with layers of hexagonal silicon sensors in the highest radiation areas and plastic scintillator tiles where radiation is lower. The detector will also be highly granular, with more than 6 million readout channels. The frontend electronics for the silicon section are separated into several physical boards. The "hexaboard" holds the HGCROC ASIC, which measures and digitizes the charge deposited in the silicon sensors, and provides a precise measurement of the time of arrival. The data are then transmitted to the concentrator ASICs via 1.28 Gbps serial links for either trigger primitive generation or data acquisition. From here the compressed data are then forwarded, still via 1.28 Gbps links, to the lpGBT, which is hosted on the "engine" boards. There, the data are serialized and sent to the off-detector readout via 10.24 Gbps links through the VTRX+. Each engine board is connected to up to 6 hexaboards via the "wagon" boards. The precise mapping is nontrivial, since each layer in the detector is different, and occupancies vary strongly both within and between layers. As a result, wagon boards come in many varieties. These electronics must all be able to withstand the radiation levels present in the detector. The ASICs are designed to handle the 1x10^16 neq/cm2 present in the inner parts of the detector. However, the VTRX+ and the bpol12V DC/DC converters used for powering, cannot withstand this level and must be placed at larger radius. An additional challenge to the electronics design is the limited physical space along the z-direction. The engine and wagon boards, along with the DC/DC board, must all fit within a 5mm wide gap between the hexaboard and the cover plate, which places constraints on board thickness, connector stacking heights, and inductor coil dimensions. This presentation will cover the recent progress made for these frontend readout electronics. A first test system has been produced that links together an engine with two wagons and five hexaboards, using an FPGA-based emulation of the concentrator ASIC and a ZCU102 as backend system. We will discuss our experience establishing full system communication and will report on signal integrity studies.

Primary author: STROBBE, Nadja (University of Minnesota (US))

Presenter: STROBBE, Nadja (University of Minnesota (US))

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