

# Upgrade of the RPC detectors' data collection and transmission electronics for the ATLAS experiment at High Luminosity LHC

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RPC detectors are used to trigger muons in the ATLAS Muon Spectrometer barrel region. The foreseen HL-LHC operation imposes replacing their trigger and readout electronics with a data collector and transmitter (DCT) system, which implements the LPGBT optical link to handle data bandwidth up to 10.24Gb/s. A testing system will be implemented to assess all DCT prototypes and mass production. Since the first DCT prototype is under irradiation tests, a methodology has been developed that renders feasible indispensable implementations towards the complete validation of the functionalities of the DCT and of any board that implements the LPGBT.

## Summary (500 words)

The HL-LHC accelerator will have an instantaneous luminosity 5-7 times above its reference value resulting in higher data rates and radiation levels that will pose significant challenges to both the experiment's detectors and the readout and trigger electronic systems.

To preserve the acceptance of critical signatures for physics, the trigger system of the ATLAS experiment has to maintain both low-momentum trigger thresholds and manageable trigger rates. Hence, it will undergo a decisive upgrade (Phase II upgrade) by increasing the trigger rate and latency to 1MHz and 10 $\mu$ s, respectively, so that more complex trigger algorithms than in the present system can be feasible[1]. That trigger scheme renders the current readout and trigger electronics, which accommodate a maximum rate of 100 kHz with a maximum latency of up to 3  $\mu$ s, incompatible.

This paper refers to the Phase II upgrade of the trigger system (based on RPC technology) in the central region (barrel) of the ATLAS Muon Spectrometer, a detector that will play a vital role in the full exploitation of the HL-LHC physics potential. It will focus on the high-radiation resistant Data Collector and Transmitter (DCT) boards that will replace the on-detector readout and trigger electronics of the RPC detectors.

The design architecture of a DCT prototype currently being under irradiation tests is presented (Figure 1). It is based on a Xilinx Artix FPGA able to digitize 288 input signals and the radiation-tolerant LPGBT ASIC [3]; a multipurpose high-speed transceiver developed for high energy physics experiments. LPGBT handles the transmission of timing, trigger data, monitoring, control, and data readout between the RPCs' Front Ends (FE) and the off-detectors barrel Sector Logic boards (SL) that implement the trigger and readout logic (Figure 2). With the implementation of the LpGBT, the data bandwidth that the DCTs can handle is up to 10.24 Gb/s.

Due to the importance of the DCT system, the complexity of the signals it handles, and the large number of boards required (1570 DCTs), an automated test station will be developed to evaluate the performance of all its functionalities.

Presented are the architecture and measurement results of a test bench developed to evaluate the DCT's optical link LpGBT by implementing its backend counterpart (lpGBT-FPGA core) [4] on a VC709 development board. Since the DCT prototype is under fabrication, and loopback tests of the lpGBT-FPGA are not possible (due to asymmetry of its downlink and uplink connections), the tests were performed by modifying the alternative of the LPGBT ASIC (lpGBT-Emulator), and by implementing it in a second VC709 board (Figure 3). Data integrity has been verified by transmitting fixed patterns from the modified lpGBT-Emulator to the lpGBT-FPGA core and vice versa at 10.24 Gb/s and 2.56 Gb/s, respectively (Figures 4,5).

Even though the DCT prototype is not yet delivered, the successful operation of the above testing setup renders feasible indispensable implementations towards the complete validation of the functionalities of the DCT (or of any board that implements the LPGBT).

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