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The Apollo ATCA design for CMS Track Finder and Pixel Readout at the HL-LHC

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The challenging conditions of High-Luminosity LHC (HL-LHC) require tailored hardware designs for the trigger and data acquisition systems. The Apollo platform features a "Service Module" (SM) with a powerful system-on-module (SoM) computer that provides standard ATCA communications and application-specific "Command Module"s (CM) with large FPGAs and high speed optical fiber links. The CMS design of Apollo will be used for Track Finder and pixel readout. It features up to two large FPGAs and 100+ optical links with speed up to 25 Gbps. This presentation will give updates on the design and show link quality results and power and thermal performance.

Summary (500 words)

High-performance ATCA blades are gaining popularity among high-energy physics experiments in view of the High-Luminosity LHC. The development for high-energy physics applications has proven to be challenging with many problems that need to be addressed (power, cooling, optical fiber management, communication interfaces and etc.). The APOLLO platform aims to provide a simple hardware environment and firmware and software toolkit which can be used for the development of ATCA blades. It consists of a common "Service Module" that handles standard ATCA communications as well as clock and power delivering and an application-specific "Command Module" (CM) with large FPGAs and many optical links to accommodate demanding algorithms and large data flow.

The Apollo Service Module is a standard-sized ATCA blade with a 7U x 180 mm cutout to accommodate one Command Module board. It contains standard ATCA power, communication and control infrastructure. It features a Xilinx Zynq System-on-Module (SoM) with embedded Linux OS for control, monitoring and local DAQ functions, a CERN IPMC or OpenIPMC and a Wisconsin ESM Ethernet switch. Standard commercial power entry and conditioning modules are used to deliver 12VDC at up to 30A to the Command Module.

In the CMS experiment, the Apollo platform will be used for the Level-1 Track Finding (TF) system and the Inner Tracker Data Trigger and Control system (IT-DTC). Level-1 TF reconstructs tracks from the Outer Tracker and calculate track parameters for the Level-1 trigger system. IT DTC reads from the Front-End ASIC chips and converts data into compact format. These two applications together require substantial FPGA resources, possible large power consumption and large number of optical links. The CMS design of the Apollo Command Module has the ability to accommodate one or two large Xilinx Ultrascale+ FPGAs with 4 channel bi-directional and 12 channel single-directional Firefly optical engines that sum up to 100+ optical links with speed up to 25 Gbps. We study carefully the design and performance of the board by using customized firmware to test power consumption, heat dissipation under CMS constraints and optical link integrity. This talk will discuss the results of these performance tests, design updates and future plans.

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