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The Scalable Readout System as a common initiative - a personal review

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When the RD51 collaboration formed in 2008, the community initiated efforts for a standardised common readout system, the Scalable Readout System (SRS). The APV25 chip, originally designed for the CMS silicon strip detector, was the working horse within the first decade reading out gaseous detectors. Meanwhile, the VMM chip has taken over and further ASICs were (Timepix, SiPMs) or are currently (Timepix3, SAMPA) included. The SRS found many applications, not only in its core field.

I will review the system and collaborative effort from the perspective of a user and developer involved over the last decade.

Summary (500 words)

The RD51 collaboration, formed in 2008, is one of CERN's research and development initiatives. In a community of about 450 members from 89 institutes in 31 countries, the technological development of Micropattern Gaseous Detectors (MPGDs) is advanced. Within the electronics working group, a general readout system for the whole collaboration was initiated and devised by a core team of experts: The Scalable Readout System (SRS).

Over the last decade, the basic SRS with the APV25 ASIC was further developed and other front-end chips were implemented. An ATCA version was derived and besides of many R&D projects, some experiments apply the whole or parts of the system.

Not all initiatives were successful and such a common effort had to overcome many obstacles. Still, the system became a standard in the gaseous detector community and beyond. Meanwhile, more than 100 SRS APV systems were sold via the CERN store. Both the CMS GEM and the ATLAS NSW upgrade performed their R&D with the system. Recently SRS was refurbished for the next decade with the implementation of the VMM chip. Projects to include SAMPA and Timepix3 are ongoing. There are plans to bring the SRS backend electronics to a recent technological standard.

Taking some messages from the EFCA Detector R&D roadmap process into account, in particular from the Training (TF9) and Electronics and On-detector Processing (TF7) symposia, my contribution will review the system and common effort. The mayor focus will be on the paradigm of the system as standardisation, adaptability and other factors like the influence of large projects, collaboration, compromises to make and less on technicalities of the electronics.

Having started as an inexperienced PhD student to implement the Timepix chip into SRS, then having been involved as a PostDoc in the mayor update of SRS for the upcoming decade with the implementation of the VMM chip as well as being a user of the system, I will look back on my more than ten years of experience with the system and the community. I will address the pros and cons of what stands behind SRS and outline how the system is used in Bonn.

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