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The CMS Barrel Calorimeter Processor demonstrator (BCPv1) board evaluation

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For the Phase 2 of the LHC, the central electromagnetic (EB) and hadronic (HCAL) calorimeters of the CMS experiment require a new back-end electronics for its readout. The first version of the ATCA-based blade, the Barrel calorimeter processor (BCPv1), has been developed with a large flexibility to allow evaluation of the different strategies. The performance of the optical links as well as clock distribution options are presented. BCPv1 is tested together with new Front-End and Trigger boards, as well as with the DAQ and trigger interface board, namely DTH, in order to demonstrate that it meets the required specifications.

Summary (500 words)

On the roadmap to a final hardware platform, the Barrel Calorimeter Processor demonstrator board (BCP demo) or BCPv1 has been produced and tested. This ATCA blade has been designed as a development platform that fulfills ECAL Barrel (EB) and HCAL subsystems (HB, HF, HO) as well as Trigger, DAQ and TCDS requirements in CMS. It hosts one KU115 Xilinx Kintex UltraScale and provides 56 bidirectional optical links, running any serial protocol that is synchronous or asynchronous to the LHC (˜40.08MHz) within line rates from <1Gb/s to 16Gb/s. The aim of this design was not to build a powerful processor board like the final BCP platform which will host a large FPGA, but instead to have a hardware platform flexible enough to be able to evaluate all required functions and define margins. BCPv1's board infrastructure includes: A System-on-Chip (SoC) in a Xilinx ZYNQ device based on the Embedded Linux Mezzanine (ELM) that controls the board. A ZYNQ-IPMC based on RealTime OS (RTOS) to monitor and manage the power acting within micro-seconds. An Ethernet Switch Module (ESM) to interconnect 5 ports. An FPGA fansink, I/O SMAs, and an RJ45 to make testing on the bench easy. SAMTEC Fireflys, SFPs and Jitter cleaners support the optical links. A 4x lane SSD up to 5G and 10GBASE-T PHY supports custom readout. Five BCPv1 have been produced from which three are operating at CERN performing integration tests with other prototypes for CMS and two in the USA serving more tests. All are fully functional and testing them did not reveal any major issue while minor fixes are noted to be applied in the coming next design (BCPv2). Eye scans of the optical links for all BCPv1 are presented. Compatibility with the Phase-2 DAQ and TCDS Hub (DTH) card also is presented. The successful implementations of the 15.66Gb/s flavor of SlinkRocket links for the DAQ interface and the symmetric TCLinks for the TCDS interface are shown. The distribution of the high precision "LHC"clock to the new ECAL Barrel On-Detector electronics with Jitter performance was measured. Clock jitter is critical on phase 2 EB because inadequate performance affects timing and energy resolution of Trigger Primitives. The Trigger Datapath was also tested with the BCPv1 sending data patterns to the new Trigger card (APd1) running 16.0Gb/s links using 64b/66b encoding. Finally, the BCPv1 to BCPv1 interface was also tested using the same protocol as the trigger. BCPv1 thermal measurements are presented with firmware utilizing large resources. Many firmware projects were developed in order to support these tests. In addition, a unified firmware was developed to support the CMS ECAL Barrel vertical test where the BCPv1 is accessing the new Very Front-End chip (LiTeDTU) through lpGBTs hosted in the new Front-End electronics. The BCPv1 base firmware is based on APx-FS developed for the APd1 card. It supports among others features the SF66 protocol used in the calorimeter trigger. We present the prototype BCPv1 design verification results in the ongoing CMS phase-2 upgrade project.

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