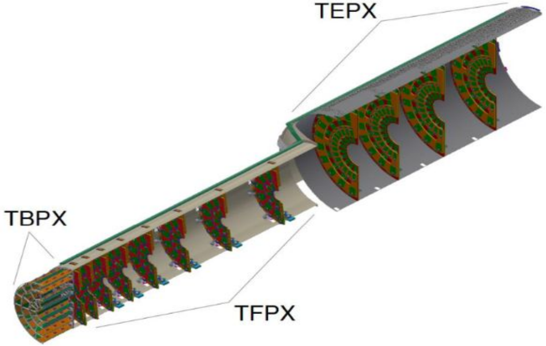
CMS Inner Tracker Electronics system development & tests

CMS Inner Tracker Upgrade for HL-LHC



- Increased granularity (x6 smaller pixels, 2500um^2)
- Increased detection coverage ($|\eta| \leq 4$)
- Reduced material budget (CF mechanics, serial powering, CO_2)
- Lower detection threshold (new readout chip)
- Simple installation and removal

- **2020/Q4: revision of the expected radiation levels in CMS. Adopted baseline:**
  - A replacement of the innermost layer/ring and portcards (optoboards) in LS5
  - Benchmark for the detector design : 1.9e16 n_{eq}/cm^2 fluence and 1.0 Grad Total Ionizing Dose

Ultimate luminosity scenario for HL-LHC (4000 fb-1)

	LHC run 4+5		LHC run 4+5+6	
	1e16 n_{eq}/cm^2	Grad	1e16 n_{eq}/cm^2	Grad
TBPX L1	1.88	1.03	3.51	1.91
TFPX R1	1.25	0.81	2.34	1.50

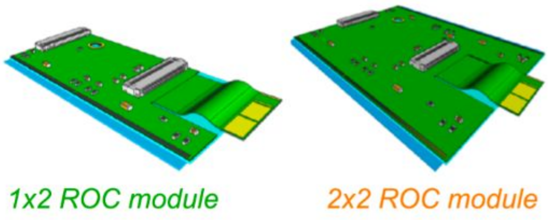
Out of reach scenario independently from the choice of the sensor technology

Inner Tracker Detector

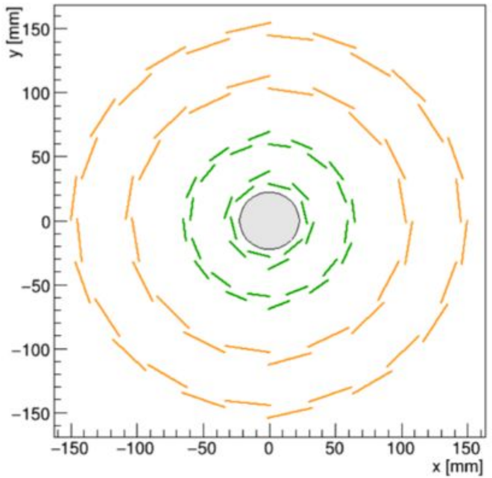
- Hybrid technology. Total active surface of ~4.9 m^2 - 3892 modules - 2G pixels

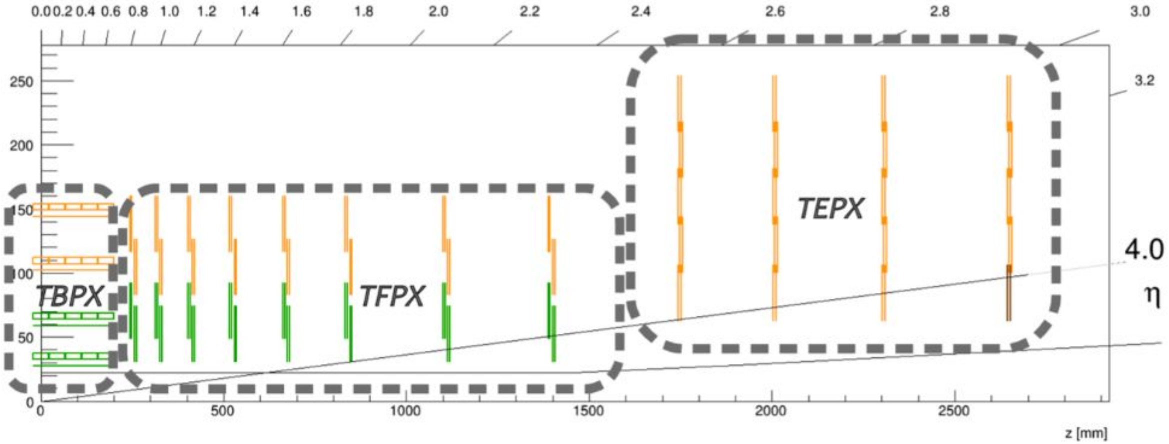
- **Detector layout featuring an extended coverage up to |η|=4**
  - 4 barrel layers (TBPX), 4 or 5 modules per ladder
  - 8 small discs (TFPX) per end, 4 rings per disc
  - 4 large discs (TEPX) per end, 5 rings per disc
  - Detector & services split in quarters (per end, per side)

- **Extra lumi triggers** for entire TEPX, dedicated TEPX D4R1 to lumi/bckgd

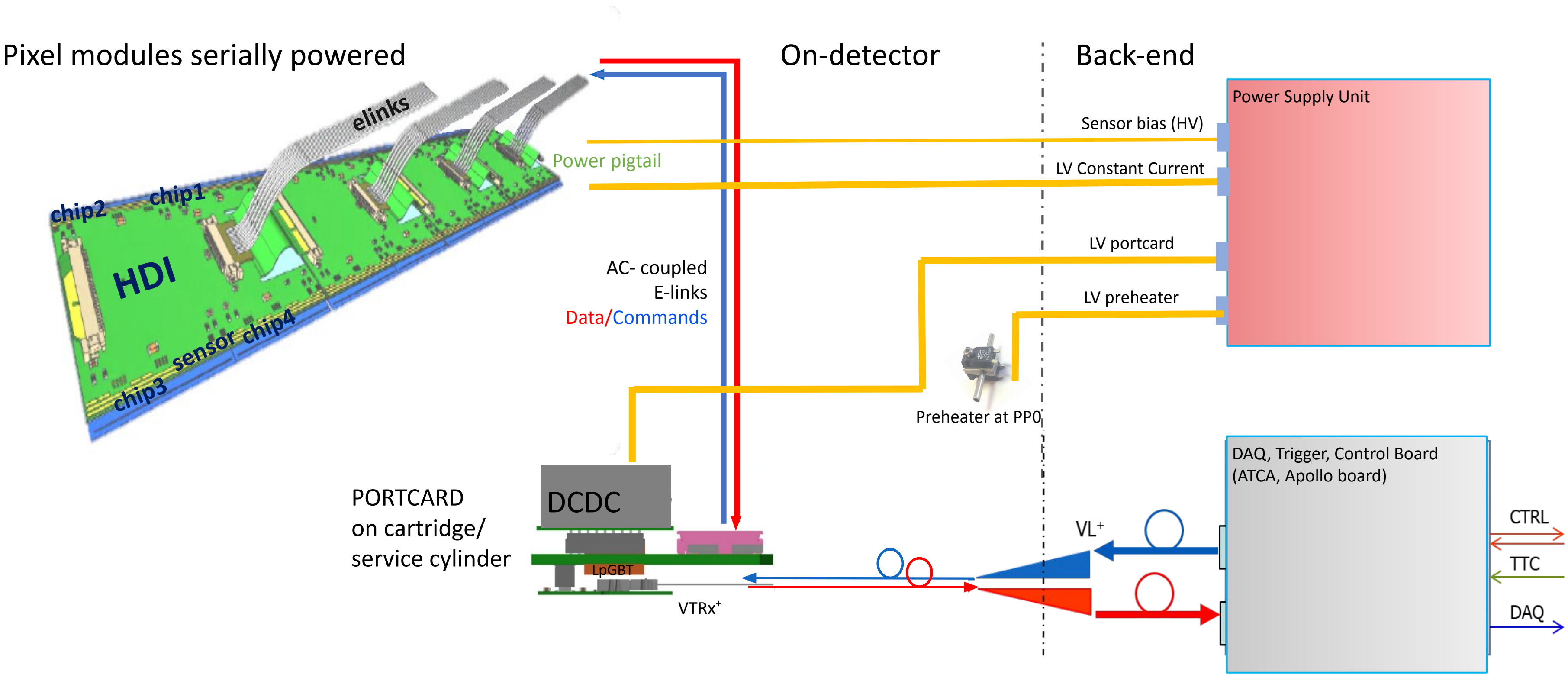


TEPX as a high-precision luminosity detector for CMS at the HL-LHC by M. Haranko
https://indico.cern.ch/event/1019078/contributions/4444412/

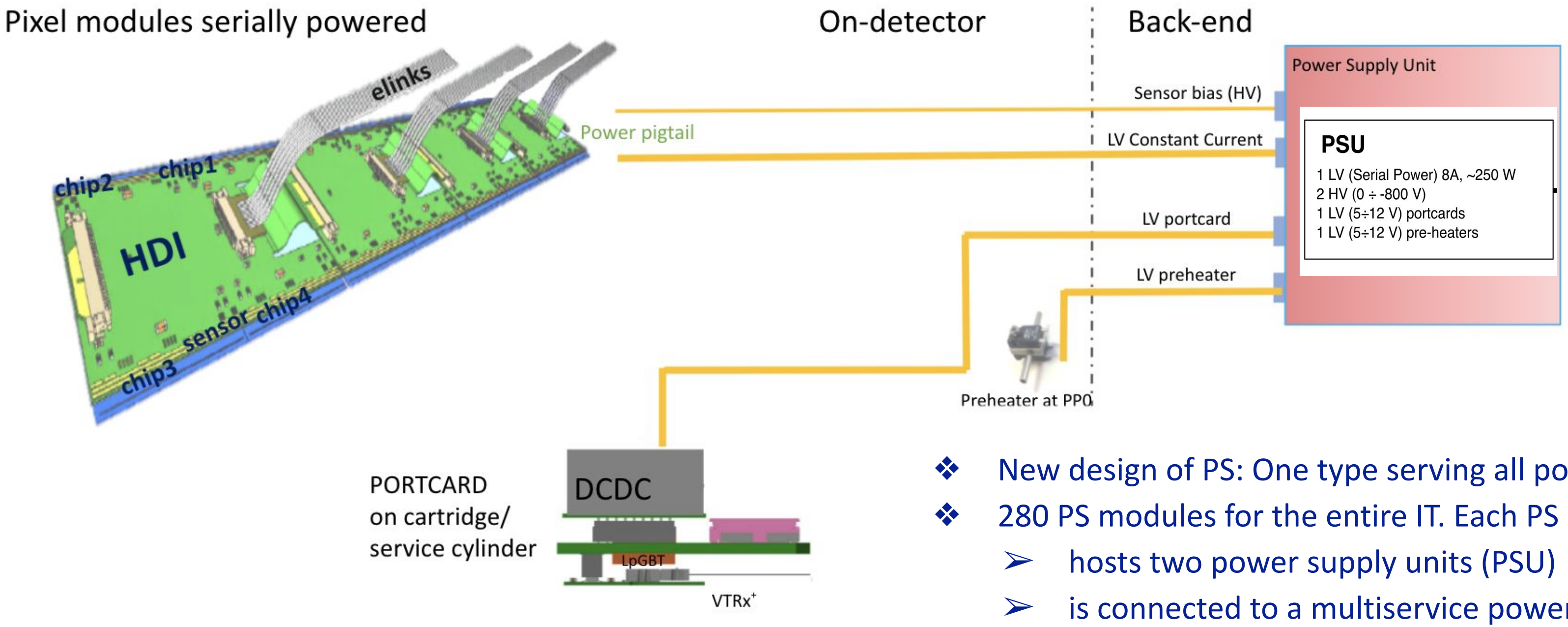




System architecture

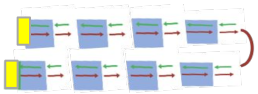


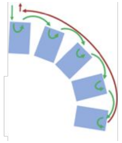
Back-end Power



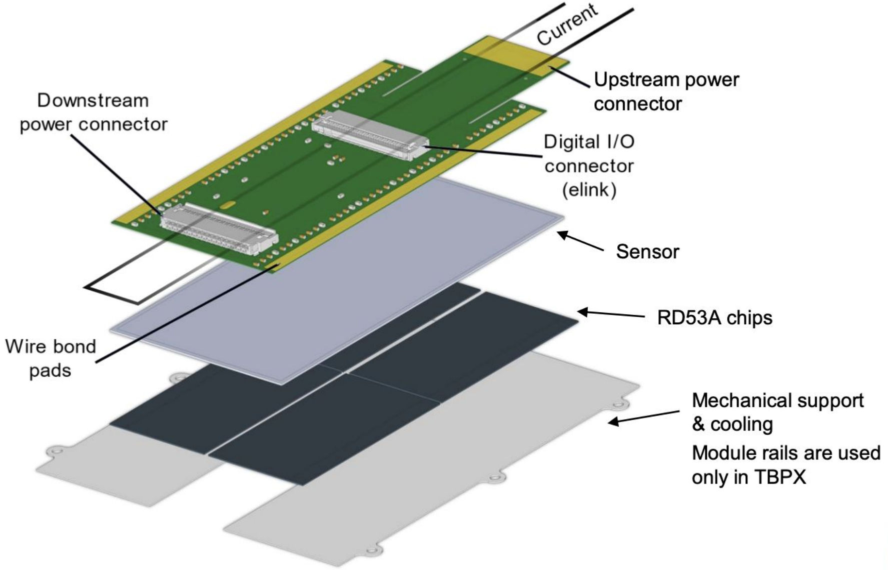
- New design of PS: One type serving all powering needs.
- 280 PS modules for the entire IT. Each PS module:
  - hosts two power supply units (PSU)
  - is connected to a multiservice power cable powering two serial power chains

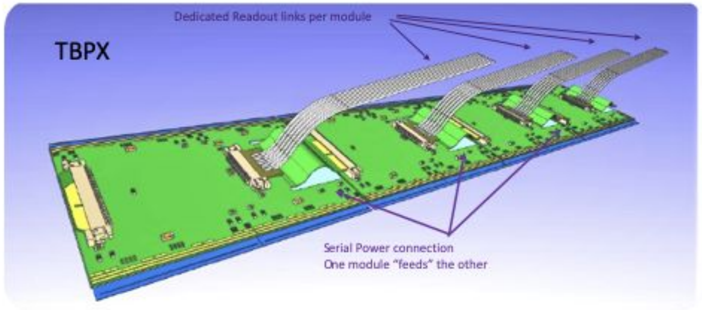
- Up to 12 modules powered in series. 500 serial power (SP) chains in the system.
- Sensor bias follows SP modularity: 1/2 HV lines per SP chain
- Portcards with 3 LpGBTs and 3 Vtrx+ powered independently by DC/DC converters
- Portcards readout modules that belong to the same SP chain (AC coupled e-links)
  - Readout follows SP modularity

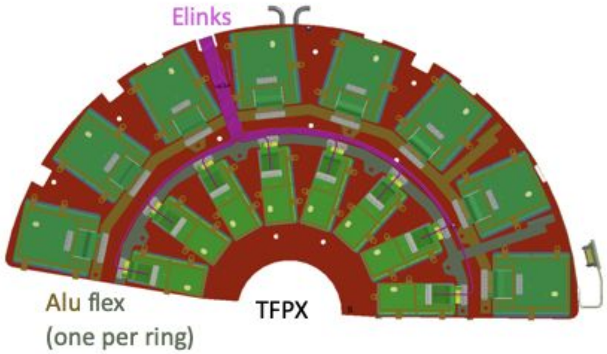


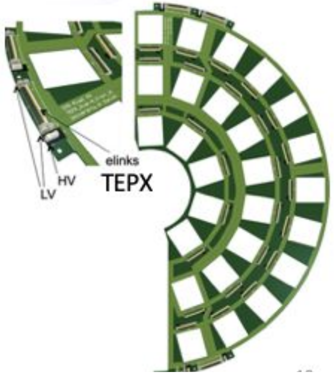


System implementation

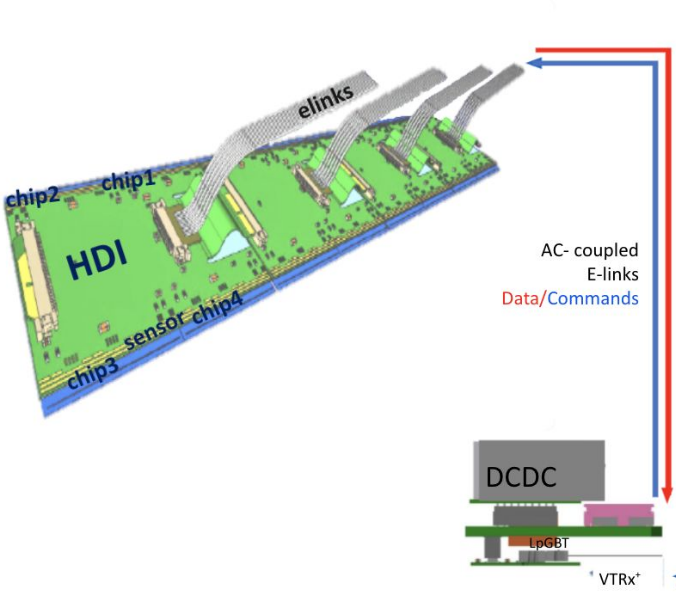




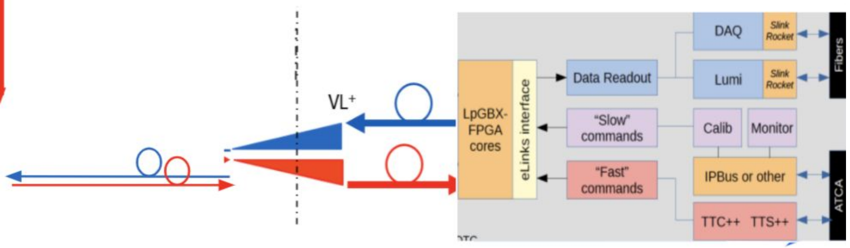




Back-end Readout



- **28 DTCs (7 per quarter) for the entire IT system**
- **Off-detector custom ATCA boards with commercial FPGAs**
  - receive triggered data & monitoring information @10 Gbps
  - send clock, trigger and configuration @2.5 Gbps
  - process two data streams: to DAQ & LUMI
- **Max aggregated compressed data b/w ~ 190 Gbps/DTC blade**



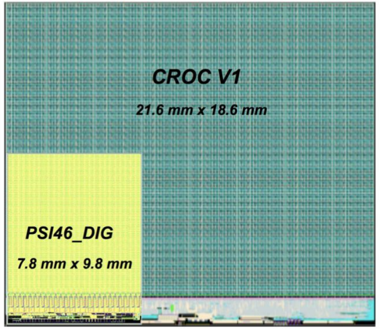
- **Up to 6 electrical up-links Aurora protocol@1.28 Gb/s per module to LpGBT**
  - Modularity depends on hit rate (location). Data merging used in the outer layers/rings.
  - Efficient data formatting to reduce data rates (factor ~2)
- **One electrical down-link @160 Mb/s per module from LpGBT**
  - Clock, trigger, commands, configuration data to modules

The Apollo ATCA design for CMS Track Finder and Pixel Readout at the HL-LHC by R.Zou
https://indico.cern.ch/event/1019078/contributions/4444412/

RD53B readout pixel chip

- **Common development for CMS & ATLAS**
  - Developed in CMOS 65nm technology within the CERN RD53 project
  - Bonding pad reticles fitting both 50x50um^2 and 25x100 um^2 pixel cells
  - Serial powering via on-chip shunt-LDO regulators (1 for analog + 1 for digital)
  - Low power consumption < 1 W/cm^2 at max trigger rate (CMS Level1: 750 kHz)
  - Radiation tolerant up to 1 Grad (verified at high dose rate), robust against SEU effects

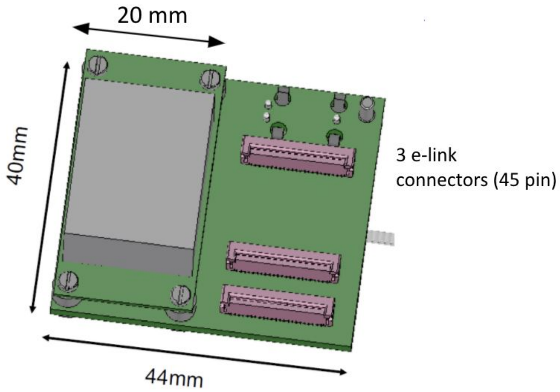
- CMS version of the ASIC submitted in June 2021, first wafers already at CERN
  - Full size ASIC: 432x336 channels
  - Chosen RD53A Analog FE linear architecture featuring an in-time threshold O(1000e)
  - 4-bit digital readout with selectable 6-to-4 bit dual slope ToT mapping to optimise resolution and range

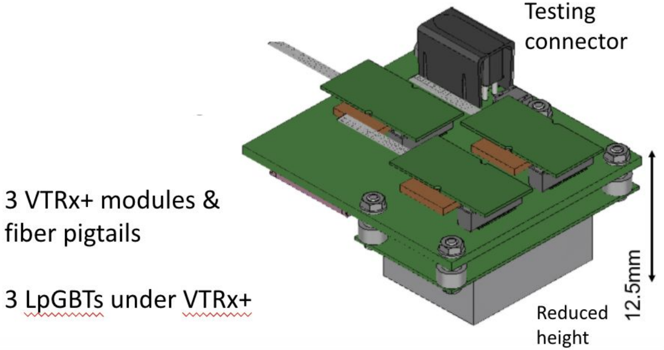


-Performance simulations and characterization of RD53 pixel chips for ATLAS and CMS HL-LHC upgrades by A.U.Rehman :
https://indico.cern.ch/event/1019078/contributions/4443947/
-Test results of RD53B chips for ATLAS and CMS phase-2 pixel upgrades by D. Koukola :
https://indico.cern.ch/event/1019078/contributions/4443955/
-Radiation hardness of the ITkPixV1 and RD53A chips by M. Mironova :
https://indico.cern.ch/event/1019078/contributions/4443960/
-Single Event Effects on the RD53B Pixel Chip Digital Logic and On-chip CDR by J. Lalic :
https://indico.cern.ch/event/1019078/contributions/4444326/
-Low dose rate irradiation of the RD53A chip with Kr-85 beta source by A. Dimitrievska :
https://indico.cern.ch/event/1019078/contributions/4444329/

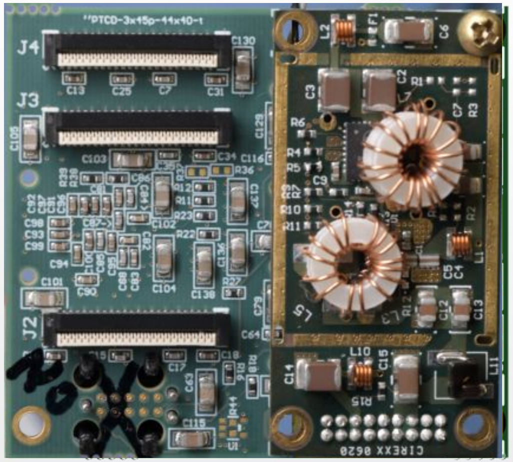
New portcard: 3 LpGBT-VTRx+ pairs (previously 2)

- **552 portcards for the IT system**
- **ONE portcard per ring <=> ONE portcard per SP chain on the disks**
- Number of LpGBTs used in the system remains the same while the number of bpols is reduced, using them more efficiently
- Design and integration of readout links and portcards on cartridge significantly easier

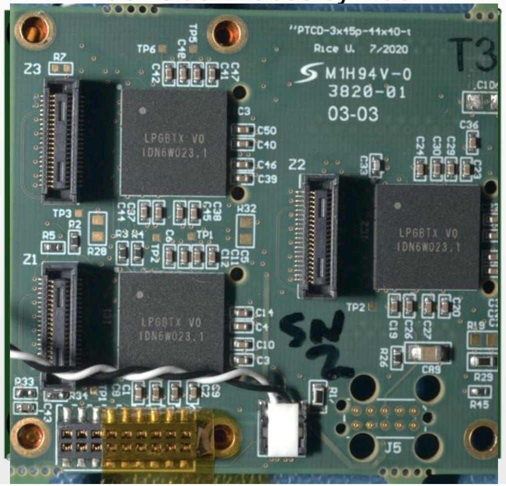




Front side – faces inward



Back side – faces cylinder



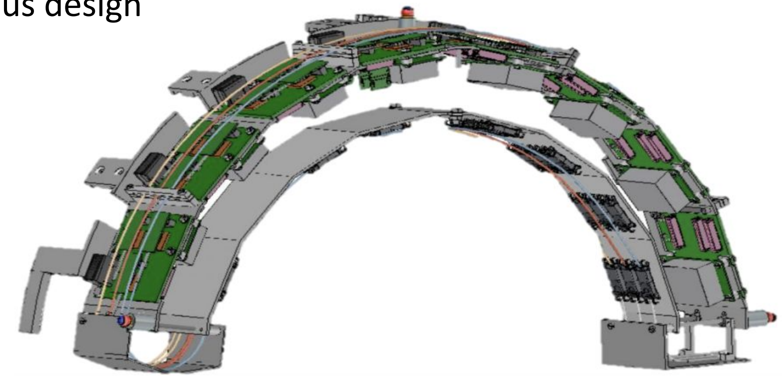
New portcard cartridge design

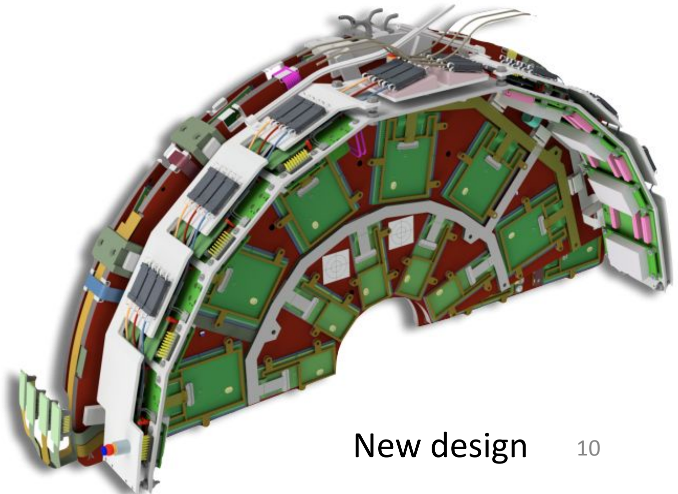
- **Portcards installed at the periphery of the disks**
  - Replacement during LS5 due to Vtrx+ and bpol radiation limits

- **Previous design was exceeding RIA specs (long fiber path over small R)**
  - Imperative to decrease the length of the fibers exposed at high doses to fit into the 1.5dB RIA budget

- **New design meets RIA budget with substantial decrease in length (x3) with some compromise in radius (~5mm) leads to a reduction of ~0.27 dB**

Previous design



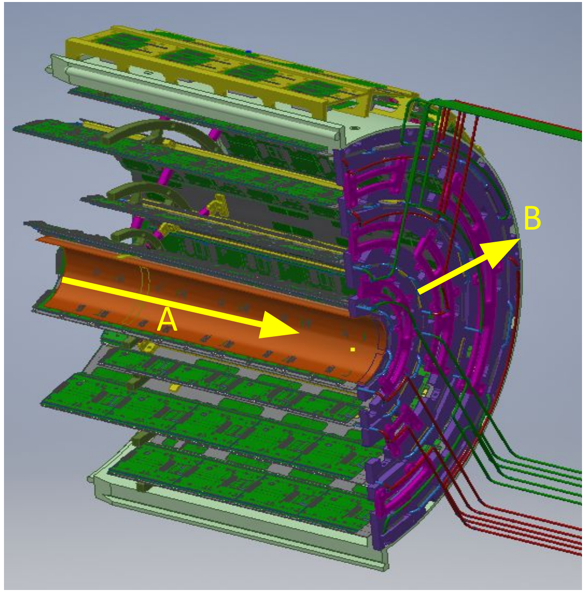


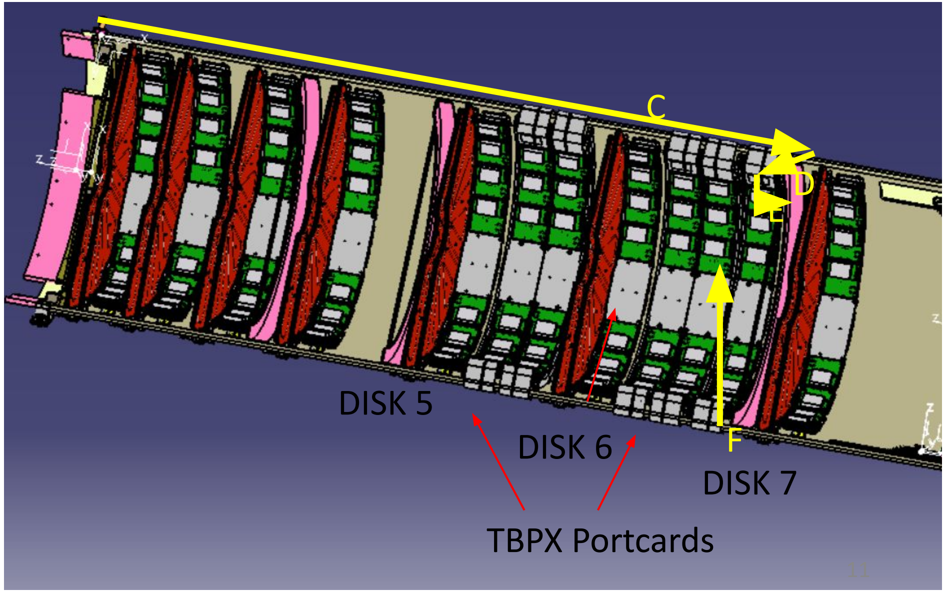
New design

TBPX Elinks & Portcards

- **TBPX Portcard: 2 cartridges between TFPX Disks 5 and 6 and 3 cartridges between Disks 6 and 7**
- **Max e-links total length estimated from CAD 1600 mm**
- Some extra length to be considered for bends
- E-links prototypes being qualified for 2 m length, to have sufficient margin

E-links path=
A+B+C+D+E+F



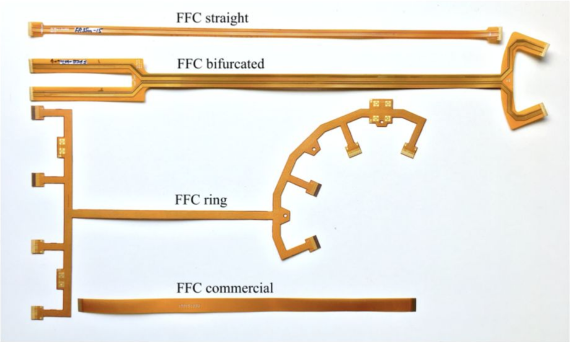


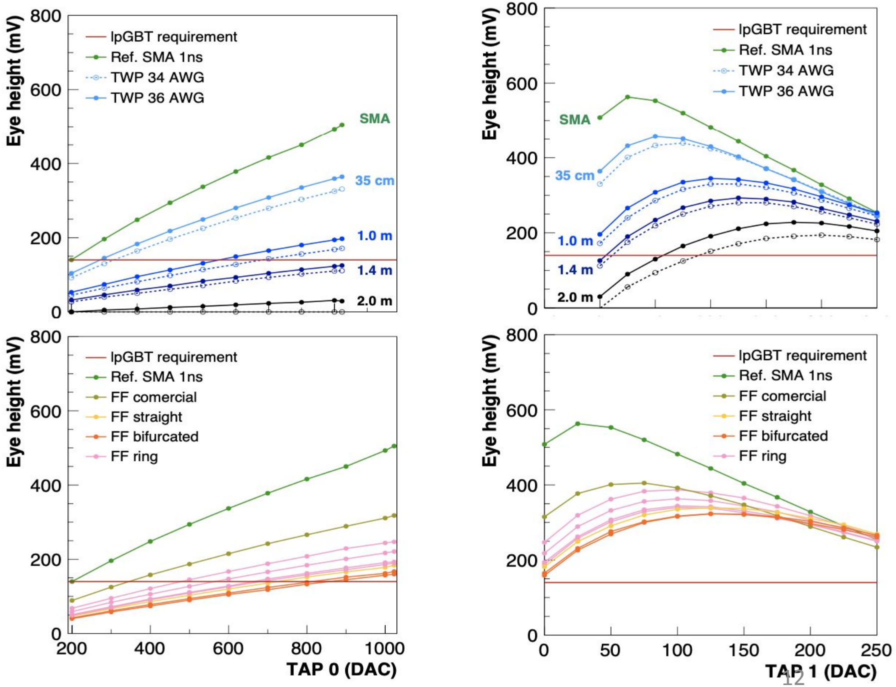
E-links development

- ~7k readout + 4k control **differential electrical links** (e-links)
- **TWP 36 AWG is the baseline**
  - Investigating flat flex solutions for ring topologies
- **Achieving required performance by optimizing the CML driver settings**
  - TAP0 sets signal amplitude, TAP1/2 set preemphasis

Twisted pair cables

Flat flex cables





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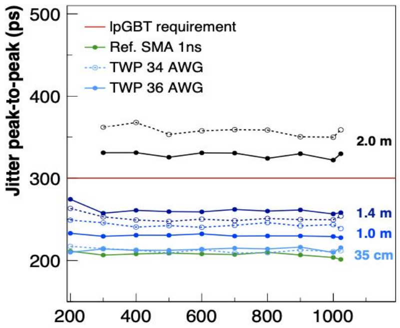
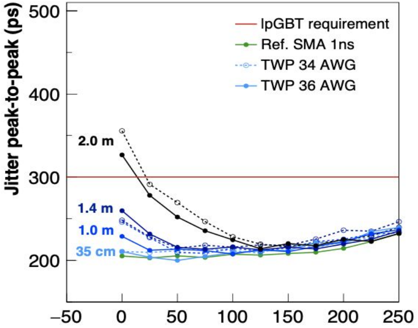
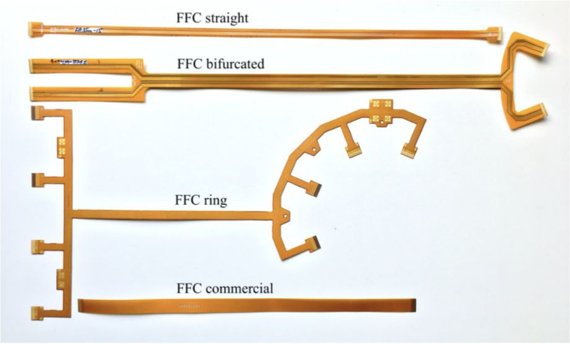
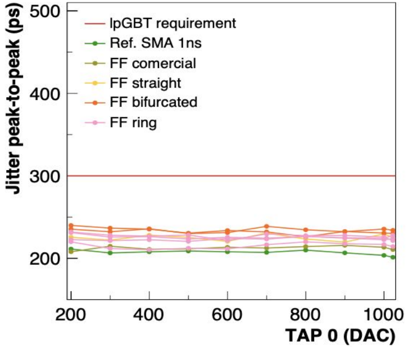
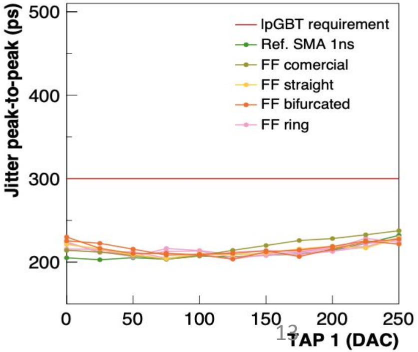






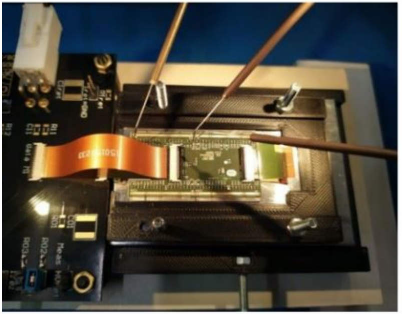
Flat flex cables





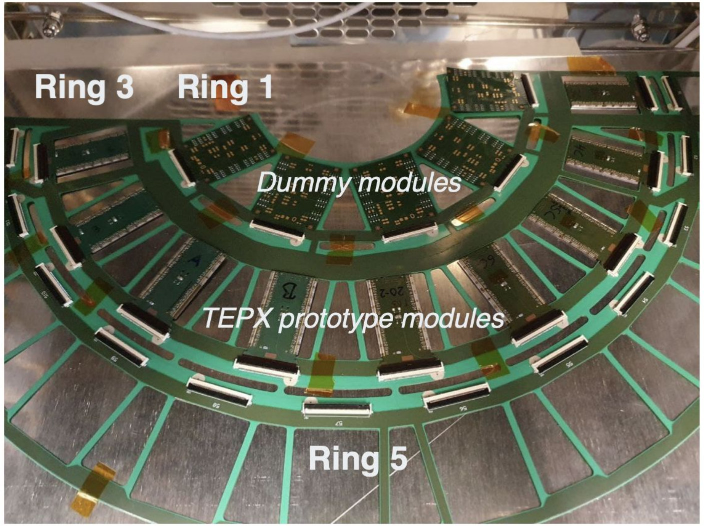
System test setups

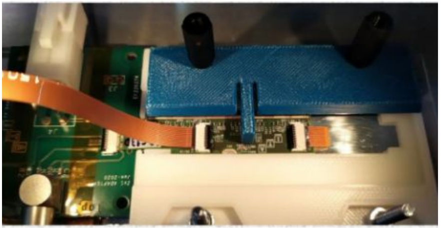
Quad module



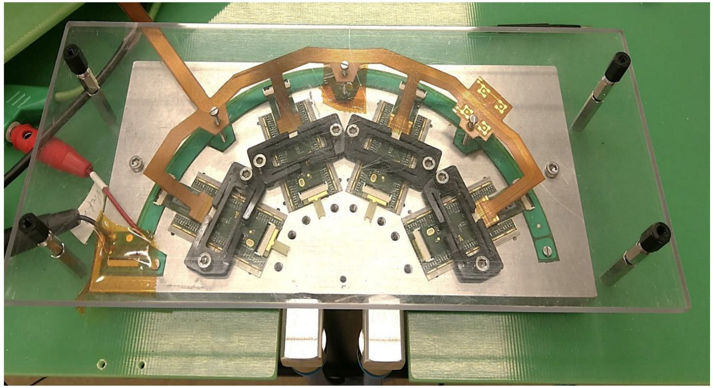
Two TBPX CF ladders readout by TWP

TEPX disk equipped with
dummy & RD53A quad modules





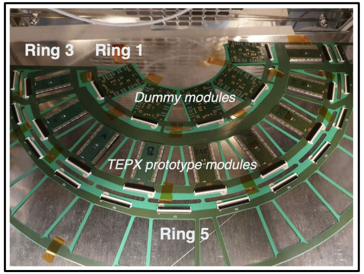
Double module

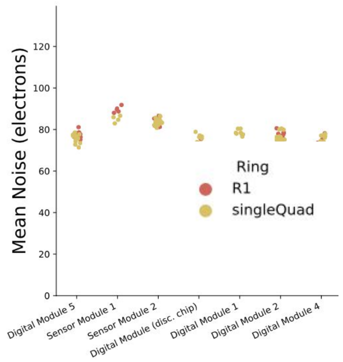


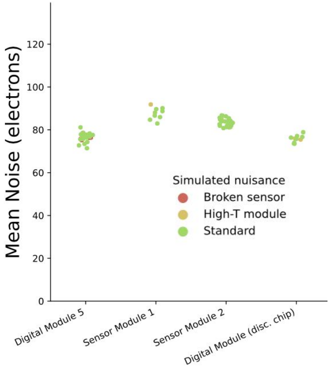
TFPX ring powered by Alu flex and readout by Cu flex

Serial Power Chain of RD53A quad modules mounted on the TEPX disk

- (Left) **Noise and width of threshold distributions compatible for standalone operation and serial powering mode**
- (Right) **No impact of broken modules on other modules in serial power chain**



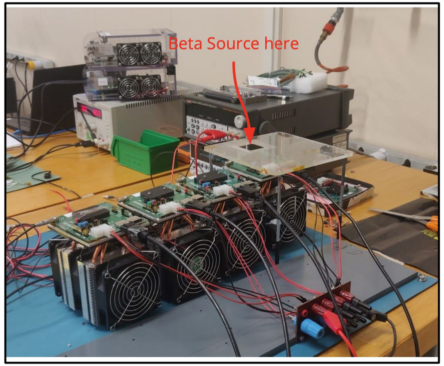




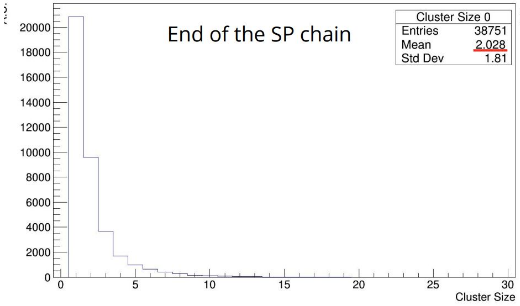
Serial powering and signal integrity characterisation for the TEPX detector for the Phase-2 CMS Inner Tracker by A. C. Reimers
https://indico.cern.ch/event/1019078/contributions/4444269/

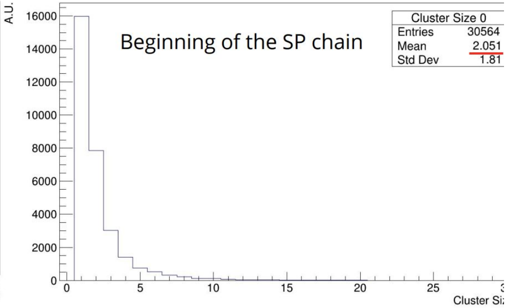
Serial Power Chain of 3D sensor modules

- 4/5 3D modules in series with the sensors sharing the bias line
- Test beam data show no performance gap for 3D modules operated between 20 V and 40 V
- ~8V maximum bias voltage drop along the serial powering chain of 5 modules
- Tested a module when placed at the beginning and the end of the chain



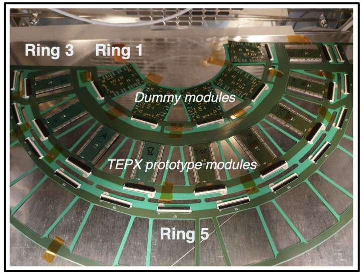
- **NO significant difference in the cluster size**

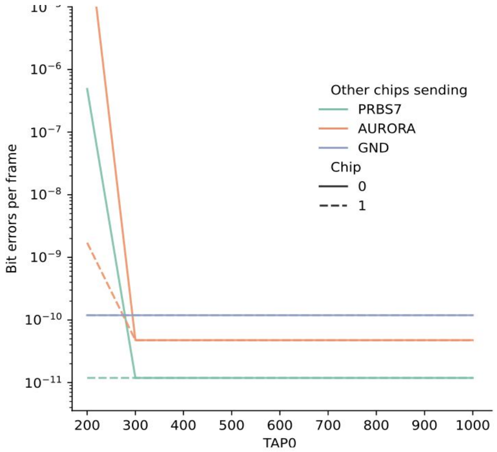




Xtalk studies of RD53A quad modules mounted on R1 of TEPX disk

- One chip per time under test, all others send AURORA, PRBS7 or GND Only very slight improvement wrt AURORA for GND and PRBS7 as expected
- **No significant crosstalk among diff. lines of disk**





Serial powering and signal integrity characterisation for the TEPX detector for the Phase-2 CMS Inner Tracker by A. C. Reimers
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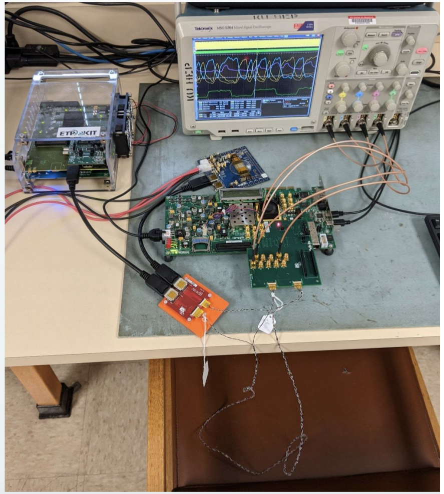
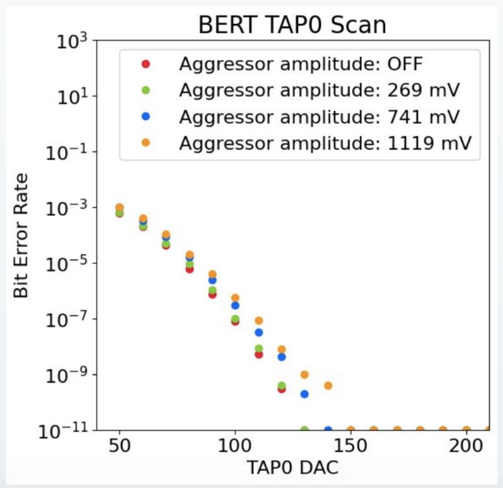
Xtalk studies among multiple TWP AWG36

- Measured the effect of external crosstalk between separate intertwined e- links. A victim e-link is connected to a RD53A Single Chip Card (SCC). The aggressor e-link is connected to a KC705 and has all four data channels sending signals.
- **Negligible crosstalk between bundles of TWP**





Development of a high bandwidth readout chain for the CMS Phase-2 pixel upgrade by C. J. Smith
https://indico.cern.ch/event/1019078/contributions/4444260/

Summary

System architecture choices for low mass services and high bandwidth readout

Recent updates of the system for optimising cost, efficiency, rad hardness

- ❖ Adopted replacement baseline scenario
- ❖ New baseline scheme fixed for one type of backend power supply for the entire system
- ❖ New portcard modularity makes disk integration much easier
- ❖ New cartridge design with significant reduction (factor x3) of fiber length exposed to high doses (less RIA)

RD53B CMS pixel chip has arrived - first wafers at CERN

Power and readout system tests performed with RD53A modules

- ❖ Serial powering tests have shown no impact on the performance of the chips/sensors
- ❖ Elinks standalone performance verified. Currently focusing on crosstalk studies.
- ❖ More system tests planned for next year with prototype modules mounted on prototype structures