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The CMS Inner Tracker electronics system development and tests

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A new Silicon Tracker will be built for the Phase 2 Upgrade of the CMS experiment. The innermost part, called the Inner Tracker, will be featuring high-granularity pixelated silicon sensors and will need to cope with extreme radiation levels and hit rates. The pixel electronics system is based on innovative solutions such as a new pixel ASIC developed by the RD53 collaboration, the novel serial powering scheme and advanced technologies for the high bandwidth readout system. The recently optimised design of the CMS Inner Tracker electronics system will be presented along with system test results with prototype components.

Summary (500 words)

A new Silicon Tracker will be built for the Phase 2 Upgrade of the CMS experiment to fully exploit the physics potential during the HL-LHC era. The innermost part, called the Inner Tracker (IT), will be featuring silicon sensors with a pixel size of $2500 \ \mu\text{m}^2$ and covering an active area of $4.9 \ \text{m}^2$. The IT system will be composed of 3892 pixel modules and the total number of readout channels will be around 2 billion.

For the ultimate HL-LHC scenario of 4000 fb⁻¹, the radiation levels will be reaching the unprecedented values of 1.9 Grad and 3.5E16 n.eq./cm² and the hit rates will go up to 3.7 GHz/cm² in the innermost layers. A simple installation and removal scheme is supported as the detector needs to be removed during each long shutdown giving also the possibility to replace and repair parts, if needed. The mass of the detector has to be as low as possible to avoid degradation of the tracking performance. These requirements pose significant challenges for the design of the electronics system. Novel solutions and advanced technologies are deployed for the design of a low-mass and radiation-hard pixel detector of high performance.

A new pixel readout chip has been designed in 65 nm CMOS technology by the RD53 collaboration. In 2021, the prototype CMS pixel chip will arrive including fixes for known bugs of previous chip versions as well as all the production required features. Serial powering will be used to power up to 12 pixel modules in series based on Shunt-LDO regulators integrated on the chips. The sensor bias will be following the modularity of the serial power chains. The pixel modules will be readout/controlled by low-mass electrical links at 1.28 Gbps/160 Mbps which will be reaching the opto-conversion boards, known as portcards. A new, optimised design of the portcard will host three pairs of lpGBT and Vtrx+ and will be powered independently by a power mezzanine with a two stage DCDC converter scheme. The portcards will be installed on a cartridge at higher radius such that their components can withstand the radiation levels. The design of this cartridge has been significantly improved in order to minimise the radiation induced attenuation along the optical fibers. A data acquisition system based on FPGA boards is developed for the back-end electronics to calibrate, control and readout the pixel modules and send the data to the central CMS DAQ. The back-end power supply system has also been greatly simplified decreasing the required design effort and cost.

In this contribution the optimised design of the CMS Inner Tracker electronics system will be presented along with system test results of serial power chains with RD53A pixel modules with sensors mounted on realistic mechanical structures, operated at cold temperatures and readout by prototype electrical elinks and portcards studying both powering and signal integrity aspects of the system.

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