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SRS-based Timepix3 readout system

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Based on Timepix3 several detector types can be built by combining it with a sensor or a photolithographically postprocessed gas amplification stage. With these combinations applications like beam telescopes and gas-based X-ray detectors can be realized.
The detectors can range from single- to multichip and from low- to high-rate applications, thus a modular and scalable system is needed. It is based on the basil framework and supports several FPGAs. Furthermore, it offers optional monitoring interfaces for detector parameters.
I will present the readout system, its scalability and how it offers the needed functionality for different detector types.

Summary (500 words)

With the combination of the highly granular pixel ASIC Timepix3 by the Medipix-3 Collaboration and several technologies like bump-bonded sensors, microchannel plates (MCP) and photolithographically postprocessed gas amplification stages (InGrid) we are developing a range of detectors. For example, we are using the combination of the ASIC and an InGrid for the development of X-ray detectors for X-ray polarimetry and for axion search at CAST and IAXO. Based on the combination of the ASICs and silicon sensors we are developing a tracker or respectively a beam telescope. The combination of the ASIC and a microchannel plate will be used for neutron detectors.
As this range of detectors has several requirements towards the readout system and a wide range of designs from low- to high-rate (Hz to MHz) and from single- to multichip, a versatile readout system is needed which adapts these applications without producing too much overhead for the others. To fulfill these requirements, we are developing a modular and scalable readout and control system based on the basil framework - a modular data acquisition system and system testing framework. The fully open-source implementation uses Verilog for the firmware and Python for the software. The system supports several FPGA boards to offer different applications a range of capabilities. One of these FPGA boards is the Scalable Readout System (SRS) by RD51 which offers scalability in low to medium rate applications. For high-rate applications we are working towards the firmware implementation on Xilinx adaptive compute acceleration platform.
Besides the scalability, the system offers an optional monitoring interface via a microcontroller for monitoring chip temperatures and power supply voltages. Additionally, further external sensors could be connected to the monitoring system for example via I^2C or SPI. For controlling the full system, the software offers a command line interface and a graphical user interface. Both interfaces also include an online event display to monitor the raw data. Additional meta data and data of the monitoring system is stored in a database and can be visualized with the monitoring tool Grafana.
This contribution will give an overview of the full system, its current state and further developments. It will be shown how the scalability and the modular design are implemented as well as how the different requirements for the applications are realized.

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