A complete readout system for the CGEM detector

Tuesday, 21 September 2021 17:44 (2 minutes)

An innovative Cylindrical Gas Electron Multiplier (CGEM) detector is under construction for the upgrade of the inner tracker of the BESIII experiment. A novel system has been worked out for the readout, including a new ASIC, dubbed TIGER, designed for the amplification and digitization of the CGEM output signals. The data output by TIGER are collected and processed by a first FPGA-based module, GEM Read Out Card, in charge of ASIC configuration and control. A second FPGA-based module, GEM Data Concentrator, builds the trigger selected event packets containing the data and stores them via the main BESIII data acquisition system.

Summary (500 words)

A ten years extension of the data taking of the Beijing Electron Spectrometer (BESIII) experiment, recently approved, motivated an upgrade program both for the collider BEPCII (Beijing Electron Positron Collider), that hosts the experiment and for some of the sub-detectors, that compose the spectrometer. The current inner drift chamber is suffering of aging and the proposal is to replace it with a detector based on Cylindrical GEM technology.

The CGEM Inner Tracker (CGEM-IT) is made of three coaxial layers of triple GEM. The tracker is expected to restore the efficiency, and to improve the z determination and the secondary vertex position reconstruction, with a resolution of 130 μm in xy plane and 300 μm along the beam direction. For the reconstruction in magnetic field with Charge Centroid and uTPC methods, it is required an analog readout and an electronics contribution to the time resolution better than 5 ns. The full system consists of about 10,000 electronics channels. The overall readout chain needs to sustain a peak rate of 14 kHz/strip of signal hits for the strips of the CGEM-IT innermost layer. In order to ensure enough bandwidth and rate capability headroom to accommodate the signal and the noise, the rate has been multiplied by a factor of safety equal to four, requesting a capability of 60 kHz/channel.

The scheme of the full readout chain is shown in the attached file.

The TIGER (Torino Integrated GEM Electronics for Readout) chips are assembled in pairs on front-end boards and installed on the detector. Each mixed-signal chip can handle the complete readout of the data incoming from 64 channels.

Data and ASIC Low Voltage are fed through Data Low Voltage Patch Cards by the GEM Read Out Cards (GEM-ROC). The core of each GEMROC is a development kit based on an FPGA of the Intel/Altera ARRIA V GX family, connected to an interface card designed for the BESIII experiment.

The GEMROC boards receive signals from the BESIII timing and trigger interface, communicate with the BESIII slow control via Ethernet interface and via optical fibers with the GEM-Data Concentrator cards, which build the events and communicate with the VME-based BESIII DAQ. The GEMROC boards manage the front-end boards power supply and configuration as well as the TIGER output data collection.

To improve the quality of the fast control signals (FCS) and overcome the signal integrity issues, an upgrade of the FCS distribution system has been designed. It consists of a System FCS Fanout module interfaced directly to the BESIII FCS, driving by bidirectional optical links four Local FCS Fanout modules. These modules use transceiver daughter cards to drive the received electrical signals onto a multi-drop backplane with single-ended signaling.

The requirements met for the CGEM-IT project make the electronics also suitable for the readout of other innovative micro-pattern gaseous detectors. It is reported how the readout system has been designed keeping in mind strong adaptability and modularity and tested using a dedicated software interface developed in Python with control, monitoring, and logging functionalities.

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Session Classification: Posters Systems, Planning, Installation, Commissioning and Running Experience

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