ZynqMP-based board-management mezzanines for Serenity ATCA-blades

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SERENITY

1 Serenity ATCA-blades

Advanced Telecommunications Computing Architecture (ATCA) standard selected for CMS Phase-2 electronics. [1]

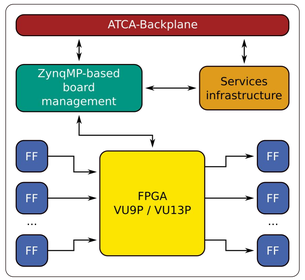
- Swappable blades in shelves
- Each blade needs IPMC and board-management
- Serenity developed for general purpose usage
- Serenity-family blades are foreseen to be used in various CMS subsystems

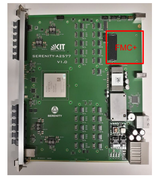
Serenity-A

- Single VU9P / VU13P FPGA
- FMC+ slot for board-management mezzanine

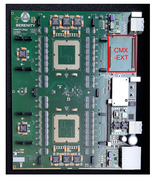
Serenity-Z

- Two Samtec Z-Ray interposers for FPGA daughtercards
  - KU15P, VU7P, VU9P, VU13P
- Extended ComExpress CMX-EXT slot for board-management mezzanine



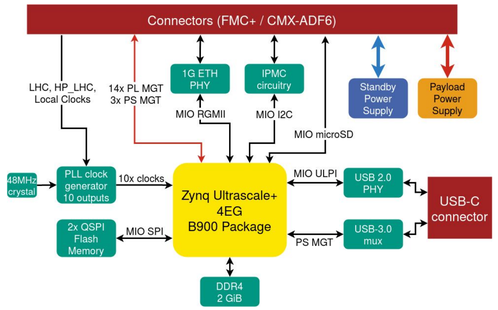


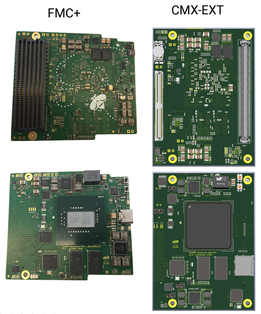
Serenity-A



Serenity-Z

2 ZynqMP board-management mezzanines





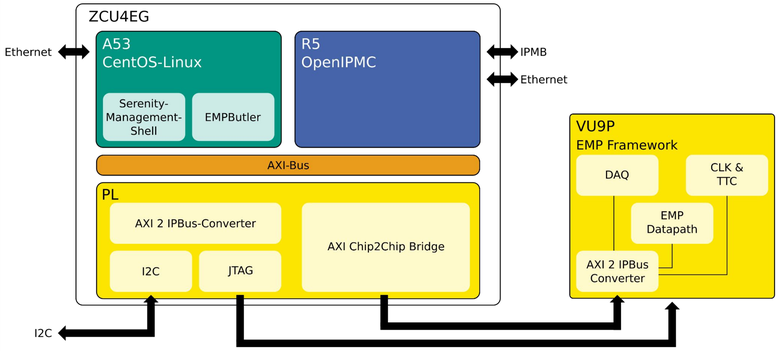
ATCA-blades needs IPMCs to communicate with shelf-manager

- ZynqMP-based board-management mezzanine can integrate IPMC-functionality into real-time cores

It is possible to either use the commercial Pigeon Point IPMC software or the open-source OpenIPMC on the Zynq Ultrascale+. [2, 3]

The CMX-EXT form-factor allows using either a commercial ComExpress module or the ZynqMP board-management mezzanine

3 Software and Firmware Framework



Programmable logic provides IPBus-connection for EMPButler and SMASH over AXI [4, 5]

- IPBus is a widely used framework at CERN
- IPBus already has many logical endpoints it connects to and software supporting it
- The EMP-framework is built with the IPBus builder

Both applications on the A53 rely on an IPBus connection:

- EMPButler
  - Registers in EMP-framework are IPBus endpoints
  - IPBus is connected via AXI Chip2Chip to AXI2IPBus converter on Virtex
- SMASH
  - I2C- and JTAG-master are IPBus endpoints
  - AXI2IPBus converter in Zynq
- Both use ipbusmmap-2.0 interface

The AXI2IPBus converter is added to linux as uio-device. This allows the applications to be run by non-root users.

Device-Tree entries for IPBus converters

```
virtex_ipbus@0xA0000000{
    reg = <0x0 0xA0000000 0x0 0x2000000>;
    compatible = "generic-uio";
    status = "okay";
    label = "IPBus on Virtex";
};
```

Connection file for the ZynqMP

```
<?xml version="1.0" encoding="UTF-8"?>

<connections>
    <connection id="virtex"
    uri="ipbusmmap-2.0:///dev/uioVIRTEX?offset=0x0
    "
    address_table="file://virtex.xml" />
</connections>
```

The main differences to using a commercial ComExpress module are:

- The FPGA is connected using AXI Chip2Chip instead of PCIe
- For the board control tasks, the glue-logic can be instantiated in the Zynq's PL instead of using an additional FPGA
- The IPMC functionality can be included in the Zynq

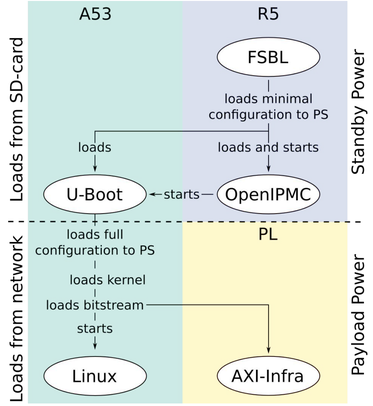
4 ZynqMP Split Boot Process

To have high maintainability, the application specific configuration of the Zynq Ultrascale+ is loaded from the network.

The split boot process has been developed to configure the PS through a network resource

- The first stage bootloader (FSBL) loads a basic configuration (e.g. DDR, Ethernet, UART) that allows the execution of u-boot with network access.
- The second stage bootloader (SSBL), in this case u-boot, loads and applies the full PS configuration.

This allows the the SoC to be mostly reconfigurable (except for parts in use e.g. DDR). [6]



5 Summary

- Two ZynqMP-based board-management mezzanines were designed for Serenity-blades in phase-2-upgrade at the CMS experiment at LHC.
- The mezzanines are available in FMC+ and CMX-EXT form-factor
- Real-time cores integrate the IPMC-functionality
- CentOS-based platform-management in application processor of ZynqMP
- PL connects applications to IPBus endpoints
- Using the split boot process, the ZynqMP-based board-management is fully configurable from the network and thus highly maintainable.

References

[1] A. Rose et.al., Serenity: An ATCA prototyping platform for CMS Phase-2, Topical Workshop on Electronics for Particle Physics (TWEPP2018), 12-21 September 2018

[2] O. Sander et. al., Exploration of ZynqUS+ for integrated slow control on Serenity for the CMS Track Trigger, CERN System on Chip Workshop, 1 July 2020

[3] A. Cascadan et. al., The OpenIPMC project, 16th CERN xTCA Interest Group Meeting, 11 May 2021

[4] A. Thea et. al., Common infrastructure F/W for Phase 2 hardware, Workshop on CMS Tracker BackEnd Systems & DAQ for Phase-2, 12 November 2018

[5] C. Ghabrous Larrea et. al., IPbus: a flexible Ethernet-based control system for xTCA hardware, JINST 10 (2015) no.02, C02019, DOI: 10.1088/1748-0221/10/02/C02019

[6] L. Ardila et. al., ZynqMP-based board-management mezzanines for the Serenity ATCA-blades, CERN System on Chip Workshop, 7-11 June 2021