Contribution ID: **20** Type: **Poster**

Design and testing of a long Flexible Printed Circuit for the ATLAS High Granularity Timing Detector

Tuesday 21 September 2021 17:46 (2 minutes)

The High Granularity Timing Detector for the ATLAS upgrade is under construction to meet the challenges of the HL-LHC. The silicon detectors along with the electronics are installed in two double-sided disks per end-cap and consist of basic units (called modules) connected to the peripheral electronics by Flexible Printed Circuit cables. The reduced space between disks and the positioning constraints as well as the large number of modules pose additional challenges for the power supply distribution and the readout system. We present the design and test results for a 2-layer flexible PCB with a maximum distance of 75cm between connections.

Summary (500 words)

The High Granularity Timing Detector (HGTD) for the ATLAS Phase II upgrade is being built to meet the demands of the High Luminosity LHC and provide a time measurement per end-cap track with a resolution of about 30 ps. This detector consists on two double-sided disks equipped with 8034 modules, two ASICs bump-bonded to two Low Gain Avalanche Detectors (LGAD) in turn glued to a flexible PCB, and is contained in a 75 mm thick vessel. The Peripheral Electronic Boards (PEB), PCBs dedicated for power and readout, surround the ring-shape active area where the modules are distributed. The interconnection between each module and the PEB is realized by a Flexible Printed Circuit (FPC), called FLEX tail. The compact design of the HGTD requires a custom design of the FLEX tail, constrained geometrically by the space available between two disks and the number of modules (220 mum thickness maximum) as well as the positioning of the modules and their connection on the PEB, defining the length. As a result, the FLEX tail length ranges from 3 cm to 69 cm. The electrical constraints are similarly challeging, including
dedicated differential pairs for signal transmission for a 1.28 Gbps maximum rate, together with dedicated lines for clock distribution and control. Moreover, planes for powering and grounding are required for the ASIC in addition to a High Voltage (HV) line to bias the LGAD sensors (800V at 3 mA). The impedance of the lines is required to be in a between 90 and 120 ohm for the differential pairs and 50 to 65 ohm for single lines for a proper impedance matching. Those constraints require a careful design, manufacturing and exhaustive testing. As part of the R&D program of the FLEX tail, a 2-layer FPC prototype has been designed and tested. The length of the prototype is 75 cm, longer than the designed length for testing purposes. It includes the lines for one module, i.e. differential pairs for communication, clock and data, single lines for control and dedicated planes for power (1.2V at 1A) and ground and a line for HV. An adapter board was designed for the FPC prototype testing. The impedance
of the differential pairs and single lines were verifed via a Time Domain Reflectometer (TDR). The voltage drop of the power and ground planes was also evaluated and compared with post-layout simulations. With regard to the signal transmission performance, a setup based on a Kintex Ultrascale+ evaluation
board emulates the realistic conditions of the FLEX tail in normal operation.The Integrated Bit Error Rate Test (IBERT) provided valuable information, having no errors detected over several days of measurement. The in infuence of the HV bias on the high-speed digital logic was also estimated. Those tests were performed at room temperature and at -30℃, the HGTD operational temperature in addition to optical tests to estimate the thermal contraction at those temperatures.

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Session Classification: Posters Systems, Planning, Installation, Commissioning and Running Experience

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