Contribution ID: **88** Type: **Poster**

# Electronics Integration for the GE2/1 and ME0 GEM Detector Systems for the CMS Phase-2 Muon System Upgrade

*Tuesday, September 21, 2021 5:48 PM (2 minutes)*

With the projected five-fold increase in instantaneous luminosity resulting from the High Luminosity upgrade of the Large Hadron Collider, the CMS experiment is in the process of upgrading its muon spectrometer. Two triple-GEM detector systems—the GE2/1, which is currently in the early mass-production phase, and the ME0, currently in the prototyping phase—are undergoing frontend electronics integration. This presentation discusses the current status of the electronics integration effort on full-size chamber prototypes by the CMS GEM collaboration, including results of grounding studies to reduce noise in the system, and the future prospects of the frontend electronics readout system.

## Summary (500 words)

With the precipitous increase in muon flux rate in the forward region of the Compact Muon Solenoid (CMS) experiment resulting from the High Luminosity upgrade of the LHC, the muon spectrometer of the CMS experiment is undergoing its Phase-2 upgrade. This talk presents the frontend electronics integration effort by the CMS GEM collaboration on two new triple-GEM detector systems for the CMS experiment—the GE2/1, which is currently in the early mass-production phase, and the ME0, currently in the prototyping phase. Specifically, we discuss the challenges of noise reduction in the GE2/1 detector system and our solution, as well as a summary of the overall status of electronics integration, aligning with the Systems, Planning, Installation, Commissioning, and Running Experience category.

The frontend electronics and their calibration and readout procedure of the GE2/1 are at relatively mature stage of development. The frontend electronics consist of a GEM electronics board (GEB) which is secured to the readout board of a GE2/1 module, and is responsible receiving the rest of the frontend electronics. These include five FEASTMP CLP DC-DC converters, 12 VFAT3 ASIC chips mounted on Plugin Cards, which connect to the readout board and the GEB, and the Optohybrid (OH) board, which is an Artix-7 FPGA-based board which serves to collect and distribute the trigger/DAQ information between the frontend ASICs and the backend advanced mezzanine card via optical signals from Versatile TransReceiver and Versatile Twin-Transmitter modules on the OH. Figure 1 displays a photo of a GE2/1 chamber instrumented with frontend electronics.

The electronics integration procedure for the GE2/1 chamber consists of tests that connect, calibrate, and program the VFAT3 ASICs. The first is a connectivity test, which establishes communication with the various ASICs on the OH and checks the functionality of the trigger links, programs the FPGA, and performs phase scans to align and program the VFAT3 ASICs with a common data transmission phase. The next procedure consists of characterizing the Digital-to-Analog Converters (DACs), with subsequent noise measurements made in two different manners: one via the data path and one via the trigger path. Figure 2 displays an example noise distribution of all 128 channels for each of the 12 VFAT3 ASICs on one GE2/1 module. This type of noise scan is used to quantify the baseline and overall reduction in noise from the various grounding schemes considered.

The frontend electronics and their integration procedure for the ME0 system are still in their infancy, but are similar to the GE2/1 detector system. This system features a GEB and plugin cards with VFAT3 ASICs. The role of the OH in the GE2/1 system is performed by the ASIC and Gigabit Optics (ASIAGO), which contains Low Power Gigabit Transfer ASICs, and transmits data via a Versatile Link PLUS to the backend. Power is provided by bPOL DC-DC converters. At the time of writing, only basic functionality tests are implemented for the ASIAGO, which are currently conducted through an adapter board, known as the Prototype Interface Mezzanine (PIZZA) mounted on a GE2/1 module's GEB.

**Primary authors:** BUTALLA, Stephen (Florida Institute of Technology (US)); HOHLMANN, Marcus (Florida Institute of Technology (US))

**Presenter:** BUTALLA, Stephen (Florida Institute of Technology (US))

**Session Classification:** Posters Systems, Planning, Installation, Commissioning and Running Experience

**Track Classification:** Systems, Planning, Installation, Commissioning and Running Experience