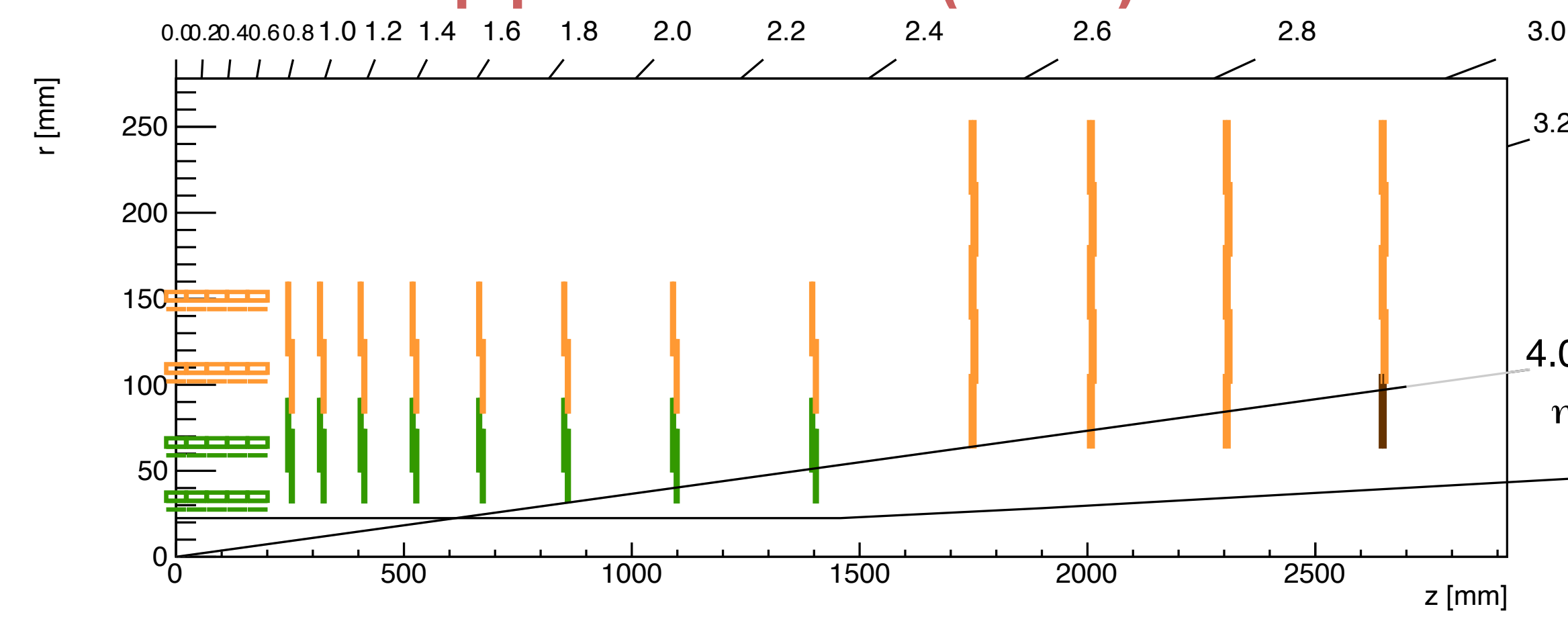


# TEPX as a high-precision luminosity detector for CMS at the HL-LHC

Mykyta Haranko on behalf of the CMS collaboration - TWEPP 2021



## 1. Tracker endcap pixel detector (TEPX)



TEPX:

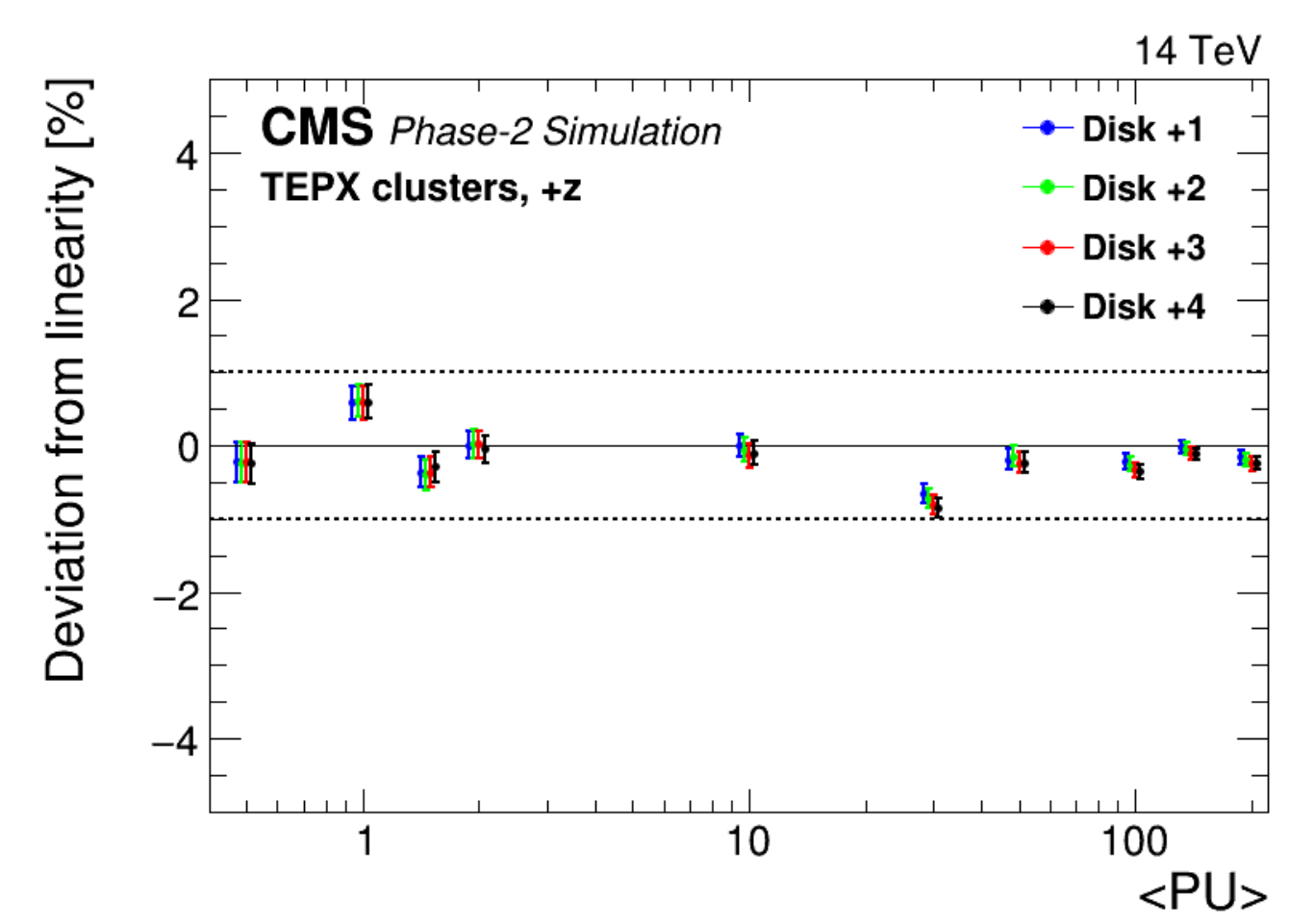
- One z-end consists of 4 double disks 5 rings each
- Is positioned at  $175 \text{ cm} < |z| < 265 \text{ cm}$ ,  $6.3 \text{ cm} < r < 25.5 \text{ cm}$  from the IP
- L1A trigger at 750 kHz is expected (for physics)
- Additional 75 kHz trigger rate for luminosity

TEPX D4R1:

- Disk 4 Ring 1 (D4R1) is beyond  $\eta = 4$  and therefore not useful for tracking
- Gets 17 ns separation between incoming bunch and collision products
- Full bandwidth (825 kHz or more) for luminosity and beam-induced background measurement

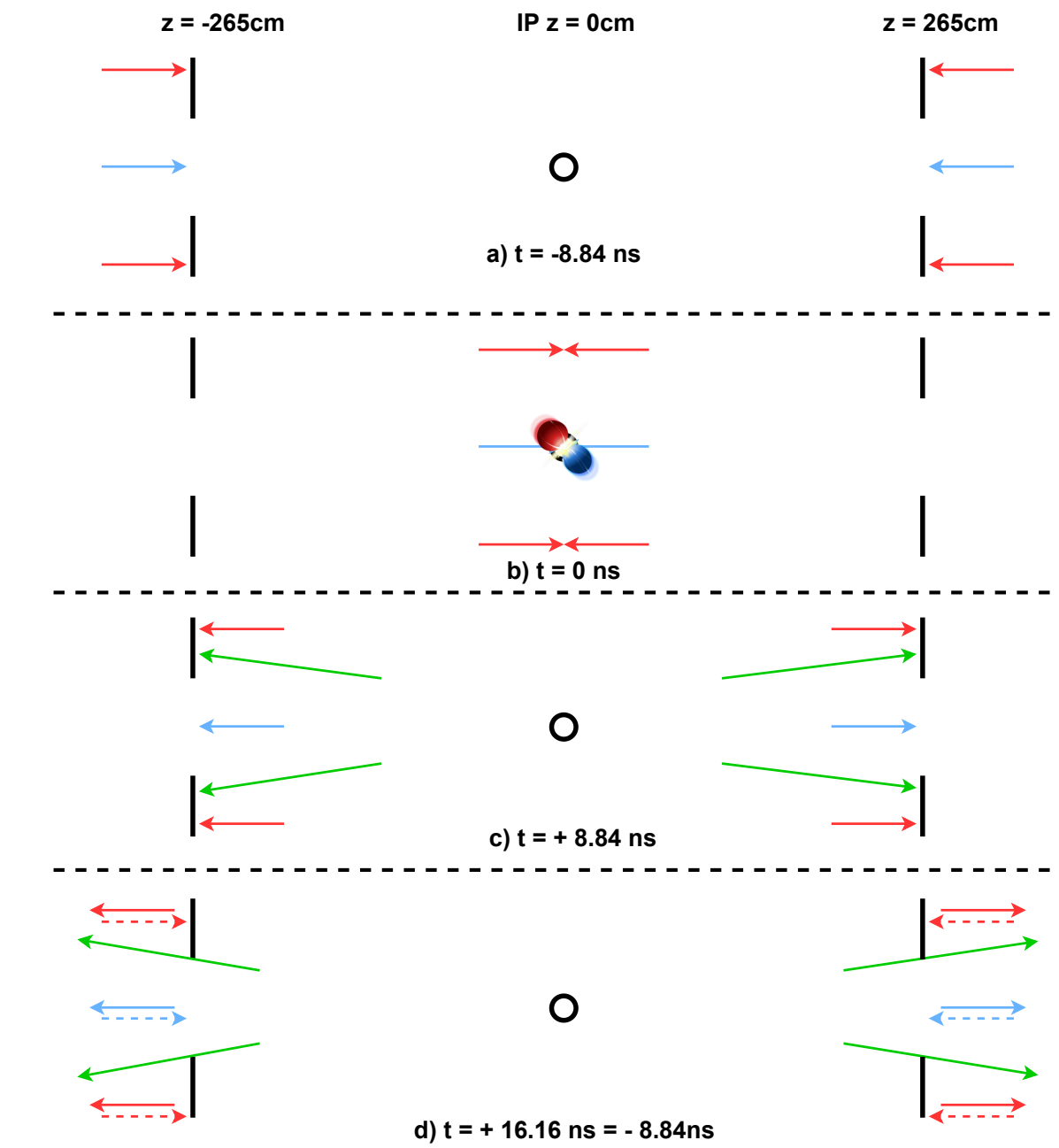
## 2. Luminosity perspective

- TEPX incl. D4R1 : (4 quarters x 5 rings x 4 disks x 2 ends) - **160 luminosity channels**
- Sampling rate (TEPX excl. D4R1)
  - 21 samples per BX per second (physics, 75 kHz)
  - 281 samples per BX per second (VdM, 1 MHz)



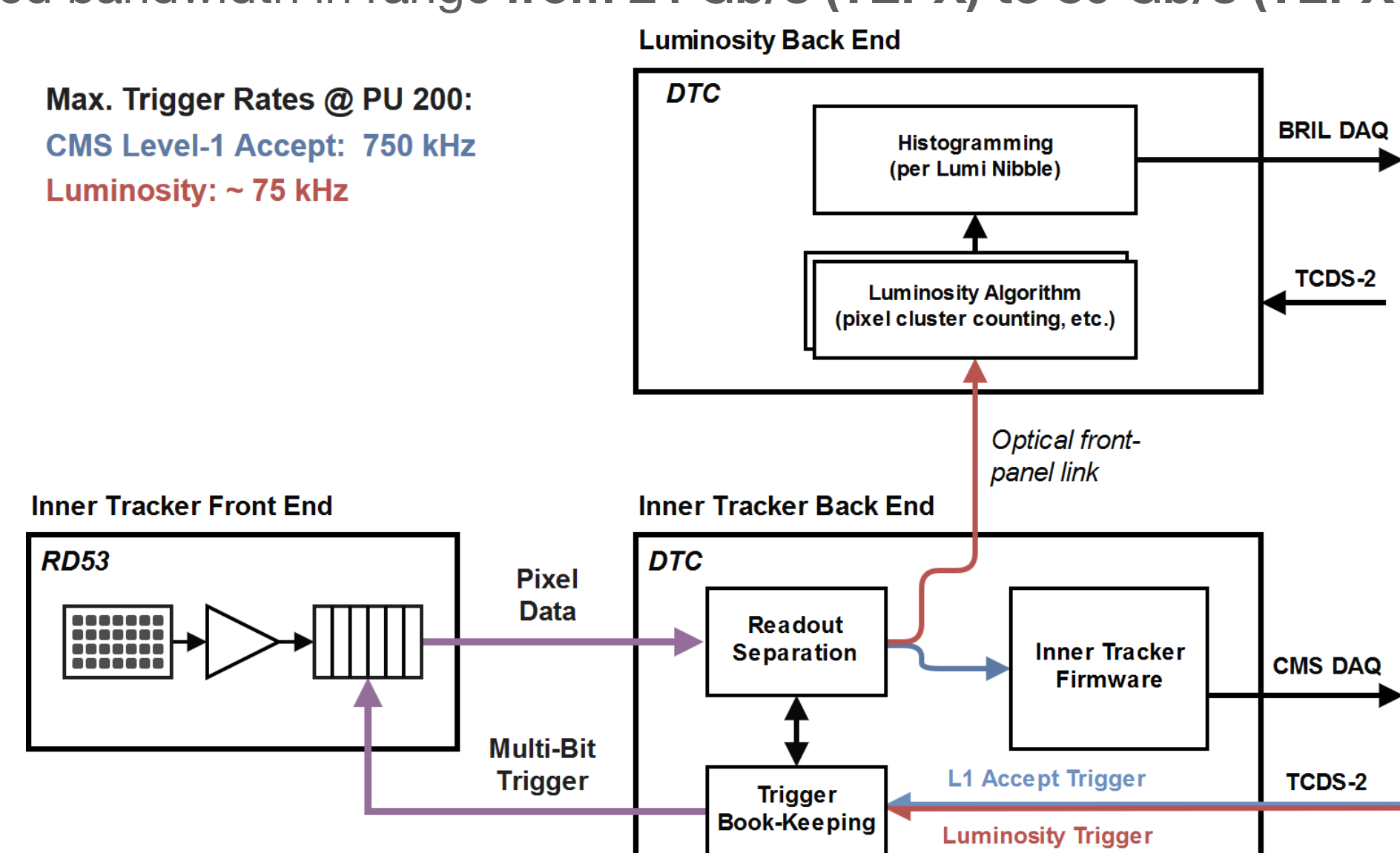
## 3. Beam-induced background perspective

- Measure before the first colliding bunch in a train (to exclude collision products and albedo)
- Appropriate time tuning to measure both luminosity and BiB



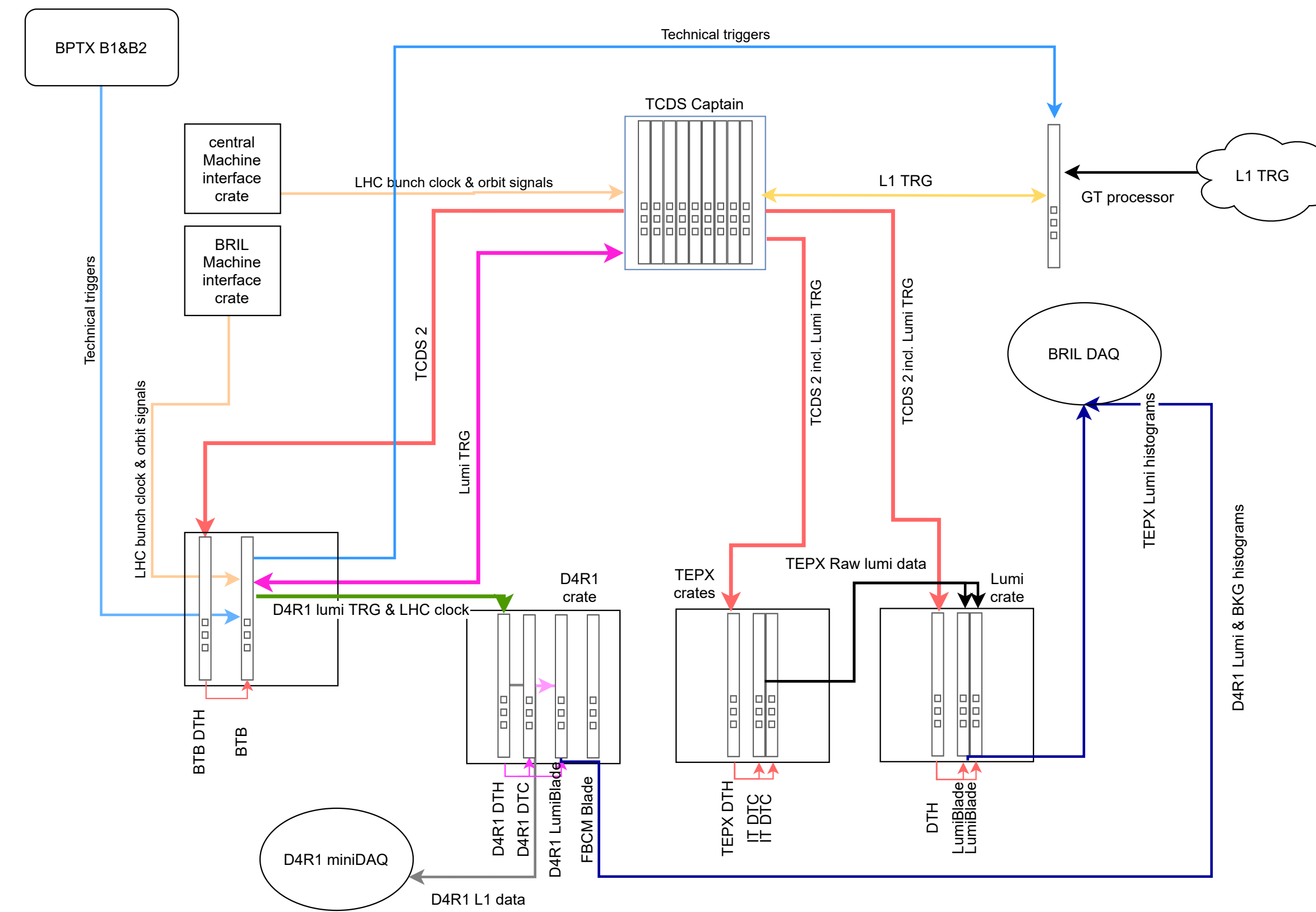
## 4. Data flow diagram

- Apollo ATCA platform will serve as both the data acquisition card and the luminosity processor
- One luminosity processor will receive data from one DAQ card
- Required bandwidth in range from 24 Gb/s (TEPX) to 80 Gb/s (TEPX D4R1)



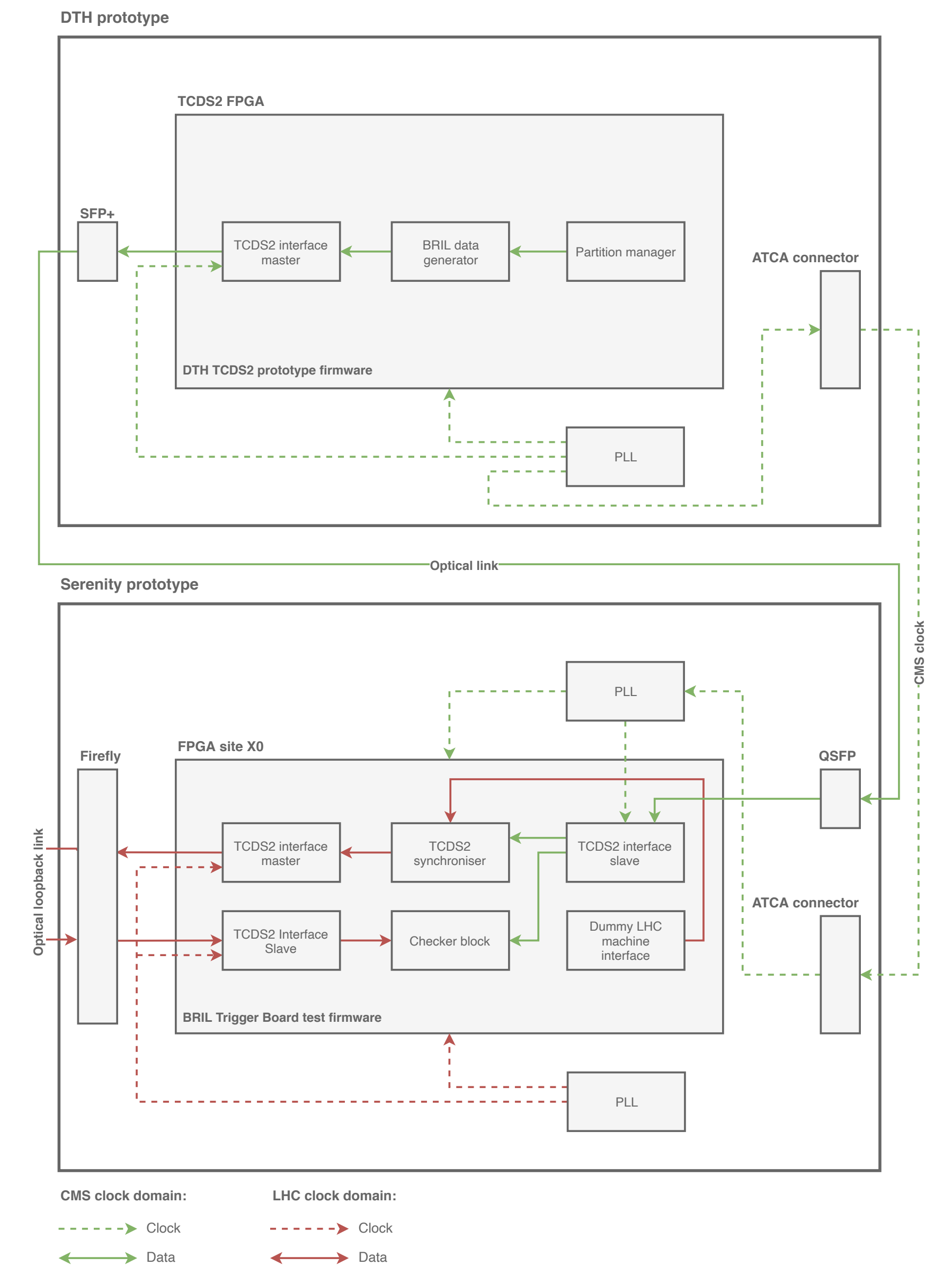
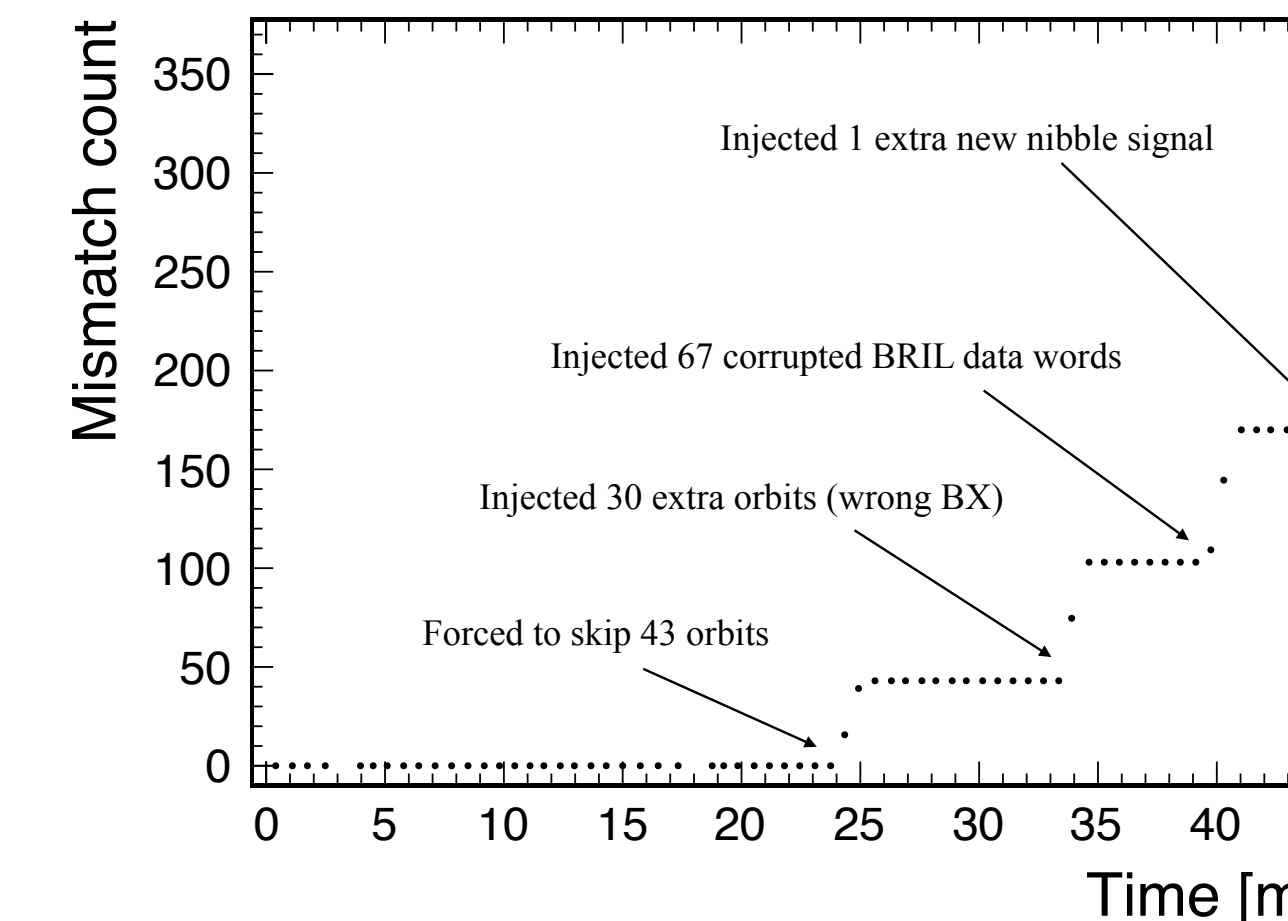
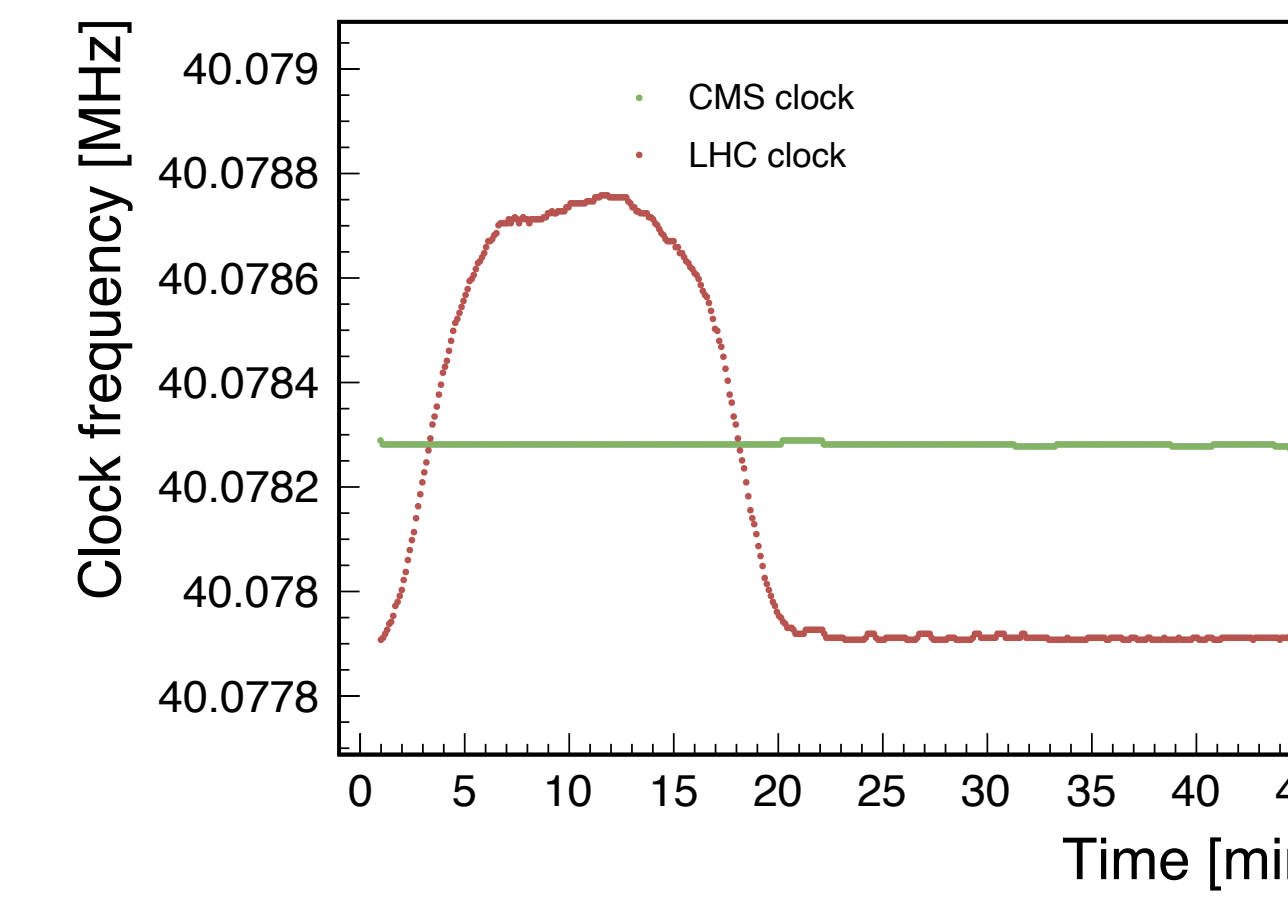
## 5. Timing and luminosity trigger distribution

- D4R1 requires dedicated clocking infrastructure to be operated when the CMS clock is not locked to the LHC clock
- In the heart of the structure - **BRIL Trigger Board (BTB)**
- BTB (based on **Serenity ATCA card**) will perform:
  - Generation of independent luminosity triggers
  - Generation of a local TCDS2-like control stream based on the LHC clock
  - Encoding of beam 1&2 signals from BPTX and transferring to the Global Trigger (GT)

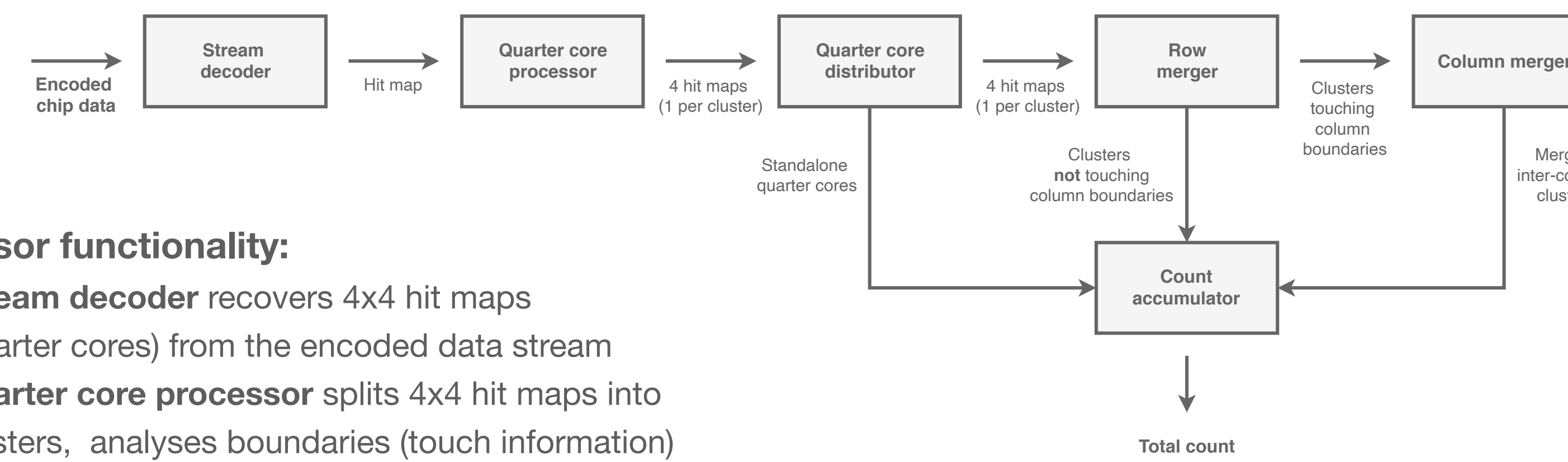


## 6. BTB proof of concept

- Utilises prototypes of Serenity and DTH boards
- Proven that the TCDS2 data stream can be transcoded into the LHC clock without issues
- Tests with the LHC ramps replayed by the PLL



## 7. Real time pixel cluster counting on FPGA - proof of concept



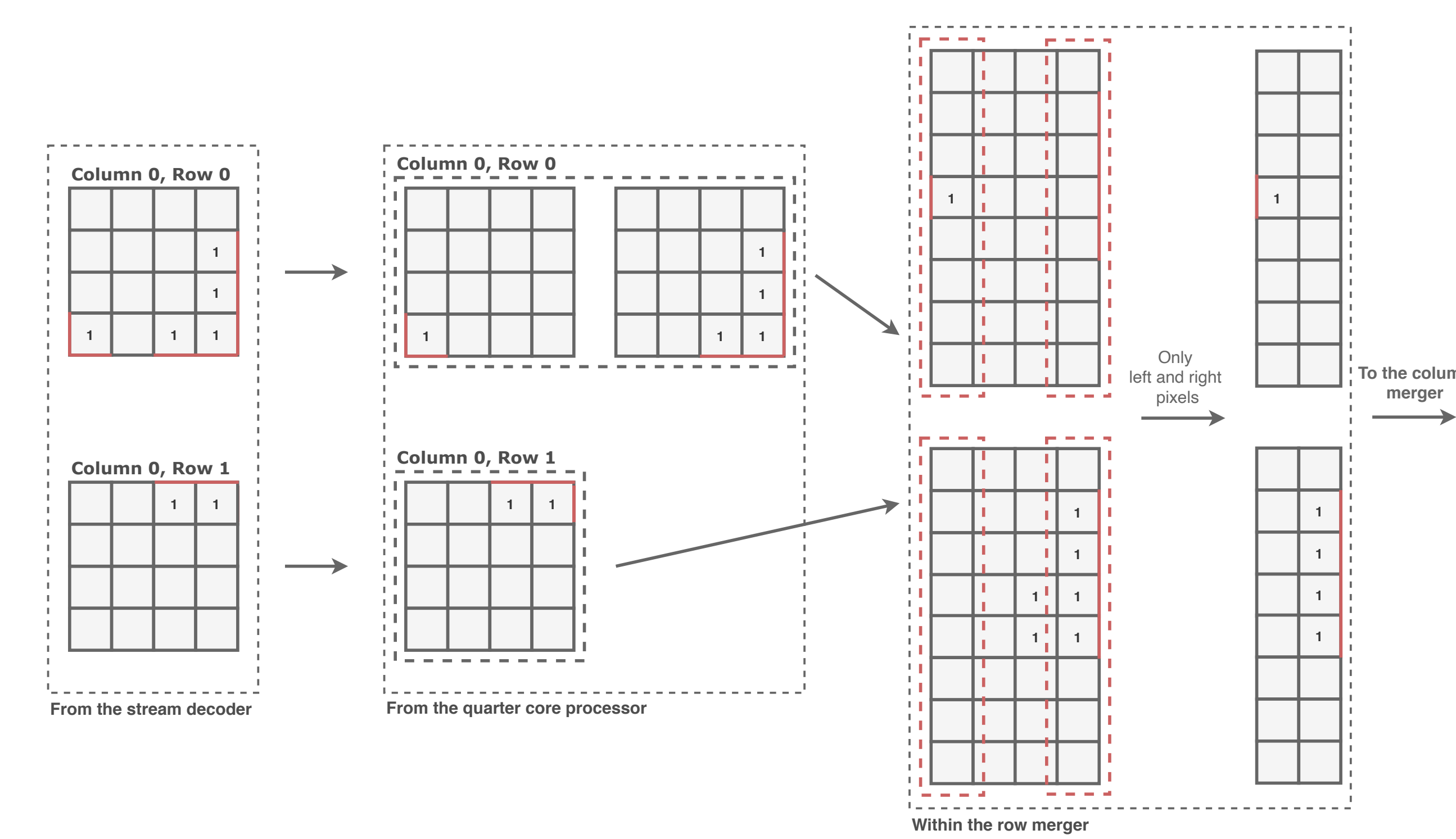
Processor functionality:

- Stream decoder recovers 4x4 hit maps (quarter cores) from the encoded data stream
- Quarter core processor splits 4x4 hit maps into clusters, analyses boundaries (touch information)
- Quarter core distributor filters isolated quarter cores
- Row merger performs vertical cluster merging
- Column merger performs horizontal cluster merging
- Count accumulator combines counts and performs status monitoring (error and warnings flags)

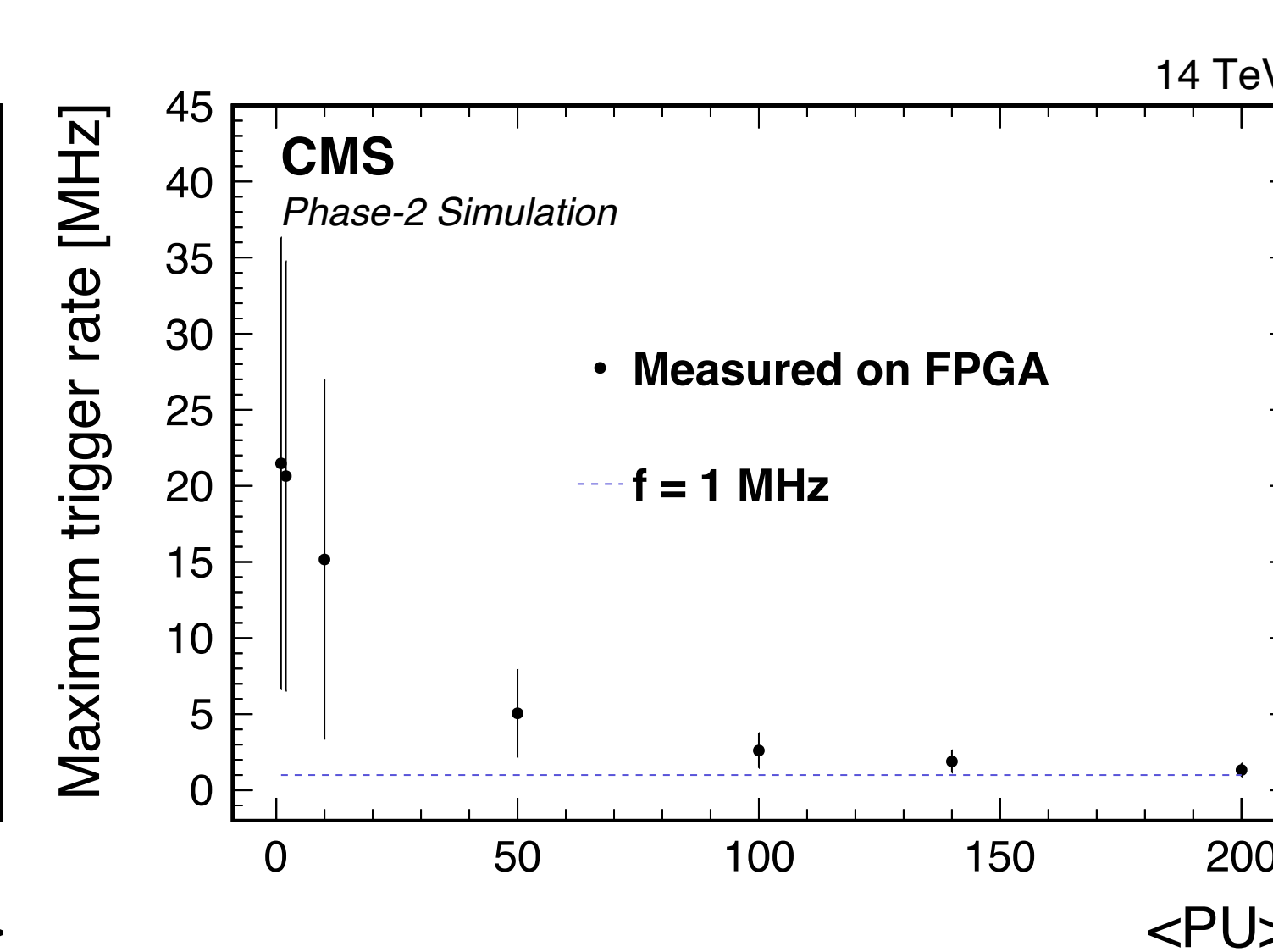
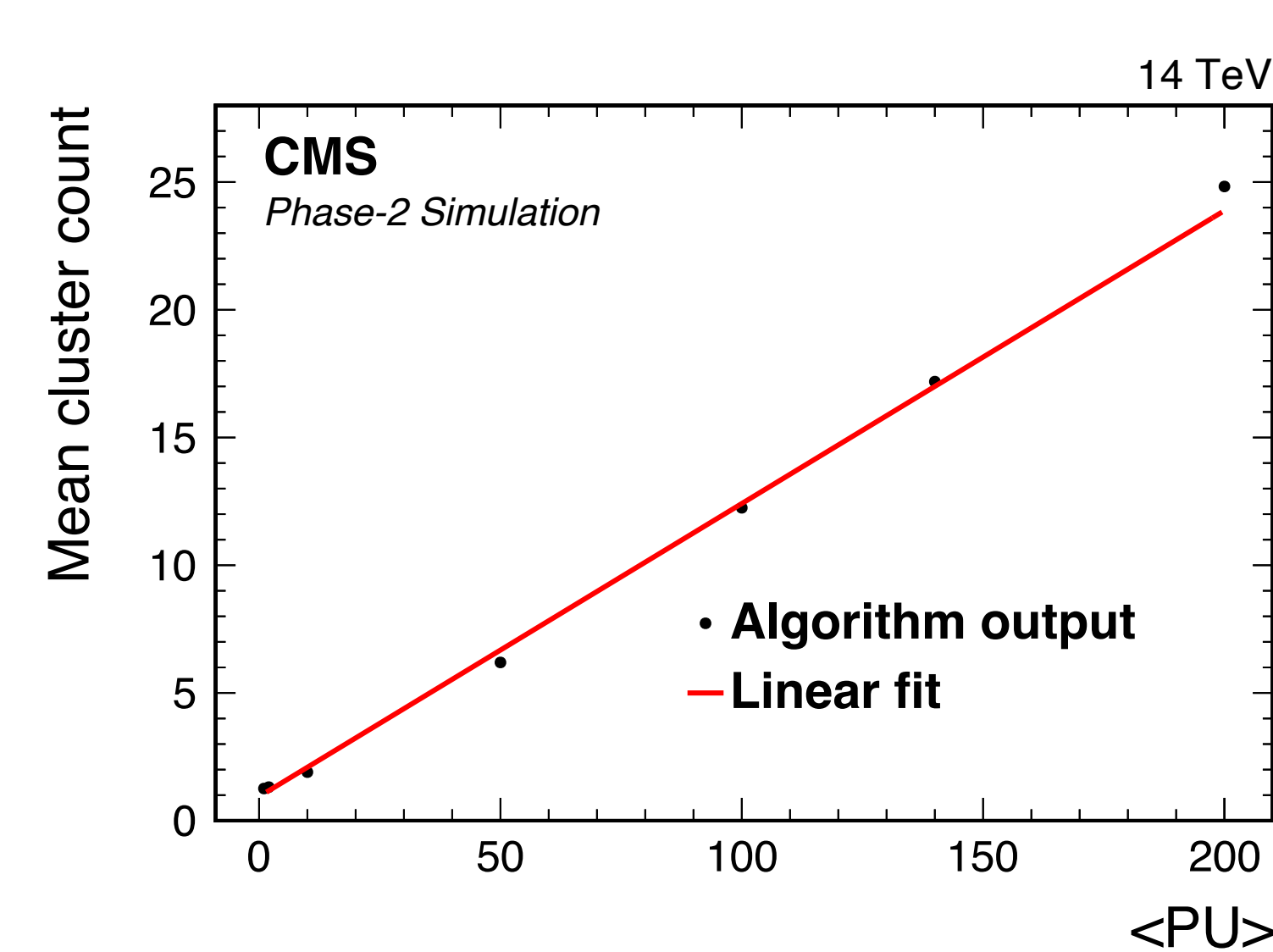
Generic properties:

- Processes raw hits per event per chip
- A set of processors running at 320 MHz
- Multiple buffering stages with configurable buffer sizes and backpressure
- Resource utilisation on VU13P for TEPX
  - 352 chips or 176 clustering instances per FPGA
  - 45% logic resources, 26% BRAM

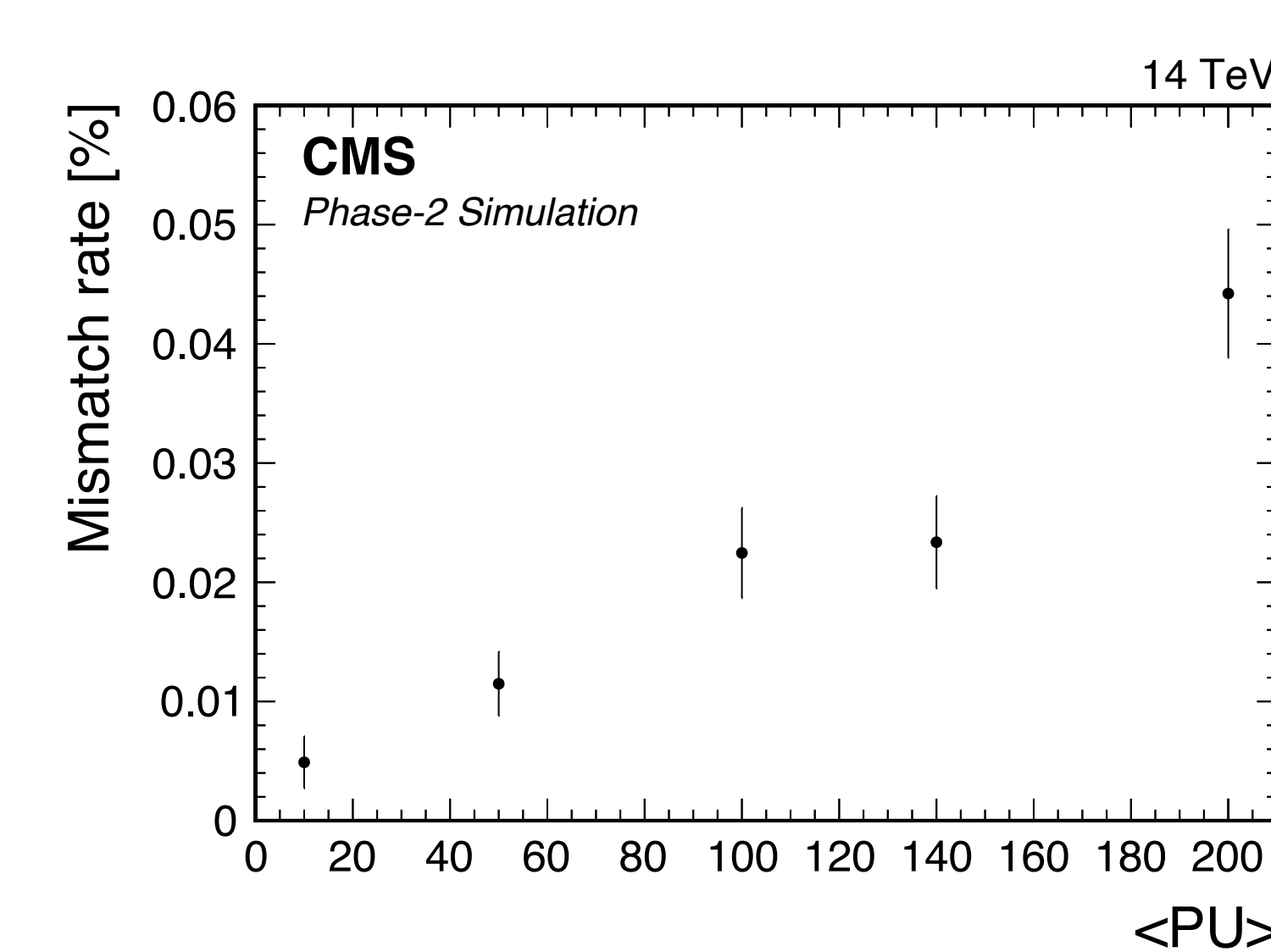
## 8. Processing example



## 9. Performance of the FPGA clustering algorithm



- Performance tested by injecting CMSSW simulated events and comparing to the offline reconstruction algorithm output



- Most of the mismatches are due to charge filtering in the offline algorithm (not available yet on FPGA)

## 10. Summary and outlook

- The developed **FPGA real time pixel cluster counting algorithm** performs extremely well and delivers cluster counts comparable to the sophisticated offline reconstruction algorithm
- The BTB proof of concept has shown the feasibility of the timing distribution architecture
- The developments are described in the **BRIL Phase-2 TDR (CMS-TDR-023)**
- Further steps are planned to study the possibility to perform ToT-based corrections and coincidence counting in overlapping regions as well as to implement the full functionality of the BTB