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TEPX as a high-precision luminosity detector for CMS at the HL-LHC

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The CMS BRIL project upgrades its instrumentation for the Phase-2 detector to provide high-precision luminosity and beam-induced background measurements. A part of the CMS Inner Tracker - the Tracker Endcap Pixel Detector (TEPX) - will allocate a fraction of the read-out bandwidth for luminometry. In the talk, the advantages and implications of the proposed approach are highlighted. A dedicated luminosity trigger distribution system is introduced together with its demonstrator system. A demonstrator of the real-time on-FPGA pixel cluster counting algorithm is also presented.

Summary (500 words)

The High-Luminosity LHC is expected to provide instantaneous luminosity a factor of five larger than provided by the existing accelerator system. This enables a higher precision for physics measurements, but also implies higher radiation levels. The precision target of the luminosity measurements is 2% real time and 1% with final calibration. In addition, the upgraded layout of the CMS Tracker also necessitates the replacement of the currently operated dedicated luminosity detectors. The BRIL Phase-2 strategy relies largely on the use of trigger primitives generated by various subsystems to measure luminosity by installing a dedicated histogramming firmware module on the back-end FPGAs. The TEPX system does not provide trigger primitives and features triggered read-out. However, TEPX modules are designed to allow a trigger bandwidth of up to 1 MHz, while physics trigger rates of only 750 kHz are expected. This allows to allocate additional bandwidth (+10% amounting to 75 kHz) to luminosity triggers. A dedicated luminosity trigger distribution system, also referred to as BRIL Trigger Board (BTB) will be built based on the Phase-2 ATCA hardware. For each group of TEPX modules, triggered luminosity data will be acquired by a back-end card and forwarded to a luminosity processor, both based on the Apollo ATCA platform. Each luminosity processor will be running an instance of the pixel cluster counting algorithm for each CMS Read-Out Chip (CROC) connected to the ATCA card. Cluster counts will be accumulated in histograms and then forwarded to the BRIL online software for final processing. This structure will allow to include TEPX in the BRIL luminosity measurement infrastructure. In addition, a part of TEPX, known as Disk 4 Ring 1 (D4R1), will not be used for tracking due to the lack of a sufficient number of tracking points and therefore will be dedicated entirely to the BRIL project. This opens a potential to use the full trigger bandwidth for luminosity measurement. The independence of the system will also allow to use it for the beam-induced background measurements even when CMS is not in data-taking mode. The latter implies the requirement for the TEPX D4R1 front-end and back-end to run during the LHC acceleration cycles, when the bunch clock frequency is not fixed. A set of tests was performed to prove the possibility of such operation, including tests of the prototype front-end modules, the back-end links and the development of the BRIL Trigger Board demonstrator firmware. In order to validate the design for real-time cluster counting with an affordable number of luminosity processors, a demonstrator pixel cluster counting algorithm has been developed and tested using CMSSW event simulations as input.

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