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A flexible and low-cost open-source IPMC mezzanine for ATCA boards based on OpenIPMC

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We present the development of an Intelligent Platform Management Controller mezzanine in a Mini DIMM form factor for use in electronic boards compliant to the Advanced Telecommunication Computing Architecture standard. The module is based on an STMicroelectronics STM32H745 microcontroller running the OpenIPMC open-source software, and its design has been published under open-source hardware license. The mezzanine has been successfully tested on a variety of ATCA boards being proposed for the upgrade of the experiments at the HL-LHC.

Summary (500 words)

Many experiments at the CERN LHC are adopting the PICMG Advanced Telecommunication Computing Architecture (ATCA) as a standard for the design of the electronic boards used in their detector back-ends. The standard requires that each board hosts a controller device, known as Intelligent Platform Management Controller (IPMC), tasked with a number of responsibilities such as managing the power state of the components of the board, measuring the health parameters of the latter and coordinating these operations together with the Shelf Management Controller. Since there are countless possibilities for the design of an ATCA electronic board, the IPMC needs to be configured specifically for the board it is meant to be used in. Therefore, an universal IPMC solution needs to be highly flexible and configurable in order to support these many different hardware configurations.

Following the success in developing OpenIPMC - an open-source microcontroller software based on FreeRTOS and implementing the IPMC features required by the PICMG standard - we developed a flexible hardware platform to serve as a host for OpenIPMC. This platform has been given the name OpenIPMC-HW.

This platform takes the form of a mini-DIMM mezzanine, pin-to-pin compatible with existing IPMC mezzanine solutions used in HEP. Similarly to the OpenIPMC software, the mezzanine design is released under an open-source license, making it very attractive for academic use in long-running experiments. At the core of the mezzanine operation lies a powerful STM32H745 microcontroller running OpenIPMC inside a FreeRTOS instance. The mezzanine has been tested and validated on a variety of ATCA electronic boards proposed for use in HEP experiments at the LHC.

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