Contribution ID: **174** Type: **Poster**

DAMIC-M electronics and acquisition system

Tuesday, 21 September 2021 18:02 (2 minutes)

We present the status of the DAMIC-M (Dark Matter In CCD at Modane) electronics and acquisition system. This first version controls a skipper CCD and measure the pixel charge with a single electron resolution. It was designed to allow optimization with respect to clocking and readout parameters to achieve the best tradeoff between noise and readout speed. We present the implementation of the full system composed of a mother board, a front end ASIC, the sequencer and ADC boards.

Summary (500 words)

The DAMIC-M experiment aims at the direct detection of dark matter particle with skipper CCDs [1] as target and sensor. Thanks to multiple non destructive charge measurements (NDCM) skipper CCDs allow to improve the pixel charge resolution from several electron to a fraction of electron (depending on the number of NDCM). The control and readout electronics have to ensure noise negligible compared to the CCD readout amplifier one (˜15nV/sqrt(Hz)) and operate at maximum speed to keep the CCD dark current as low as possible.
The V1 of the DAMIC-M electronics comprises:
- A mother with an FPGA Altera ArriaV and a complete firmware to sequence the CCD and control the board and elements below.
- a front-end ASIC that will be placed at a few centimeters to amplify the CCD video signal with the option to perform an analog correlated double sampling.
- a dedicated board to produce the CCD clocks and biases. This board integrates CABAC [2] chips with the capability of clock rise and fall time configuration.
- An ADC board, for which 3 solutions are implemented and tested with either 20bit 1.6MS/s AD4020 with LVDS interface, a 20 bit 1.8MS/s with isolated digital interface or an 18bits 15MS/s LTC2387-18.

We present the implementation of this first system, the results of test and the plan for the future version.

[1] Tieffenberg et al. Single-electron and single-photon sensitivity with a silicon Skipper CCD, arXiv:1706.00028
[2] H. Lebbolo et al. CABAC : A CCD Clocking and Biasing Chip for LSST Camera. 2013 IEEE Nuclear Science Symposium and Medical Imaging Conference, and Room-Temperature Semiconductor X-Ray and Gamma-Ray Detectors workshop, Oct 2013, Seoul, South Korea

Primary author: GAIOR, Romain (LPNHE)

Co-author: VILAR, rocio (ifca)

Presenter: GAIOR, Romain (LPNHE)

Session Classification: Posters Systems, Planning, Installation, Commissioning and Running Experience

Track Classification: Systems, Planning, Installation, Commissioning and Running Experience