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The TileCal TDAQ interface module for the Phase II Upgrade of the ATLAS Tile Calorimeter

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In order to meet the requirements for the High Luminosity-Large Hadron Collider (HL-LHC), a completely new architecture will be used to redesign the readout electronics of the ATLAS Tile Calorimeter (TileCal) system for the ATLAS Phase-II Upgrade. In the new Trigger and Data AcQuisition (TDAQ) architecture, the output signals of the Tile detector cells will be digitized in the front-end electronics and transferred for every bunch crossing to the off-detector Tile PreProcessor (TilePPr) modules through high-speed optical links. The TilePPr will then reconstruct energy deposited in each cell from the digitized samples and transfer the pre-processed cell energy data further

Summary (500 words)

In order to meet the requirements for the High Luminosity-Large Hadron Collider (HL-LHC), a completely new architecture will be used to redesign the readout electronics of the ATLAS Tile Calorimeter (TileCal) system for the ATLAS Phase-II Upgrade. In the new Trigger and Data AcQuisition (TDAQ) architecture, the output signals of the Tile detector cells will be digitized in the front-end electronics and transferred for every bunch crossing to the off-detector Tile PreProcessor (TilePPr) modules through high-speed optical links. The TilePPr will then reconstruct energy deposited in each cell from the digitized samples and transfer the pre-processed cell energy data further to the Tile TDAQ interface (TileTDAQi) modules. The TileTDAQi will then group the cell energy data to generate trigger primitives with different granularity and implement interfaces based on different requirements from the Feature Extractor (FEX) and other trigger processor modules. At the same time, the TilePPr will also store the energy information in pipeline memories and send selected data out to the ATLAS data acquisition system. The TileTDAQi module will be implemented on an Advanced Telecommunications Computing Architecture (ATCA) Rear Transition Module (RTM) format and will operate under the ATCA framework. This contribution will provide an overview of the new TileCal back-end electronics architecture and present the design and implementation of the TileTDAQi prototype together with preliminary test results.

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