The Caribou DAQ System

Current Status and Ongoing Developments

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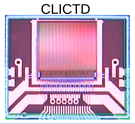
- **Motivation**: Many different silicon detector technologies under investigation
  - Similar DAQ requirements: readout, control, powering for most silicon pixel detectors
  - Differences in voltage levels, number of channels (data/voltage) or protocols
- **Goal**: Provide a versatile DAQ system which
  - Offers re-usable hardware, firmware and software components
  - minimizes device integration effort
  - reduces time to get first data from a new detector
- Open source hardware, firmware and software for laboratory and high-rate beam tests
- Developed & maintained by collective effort

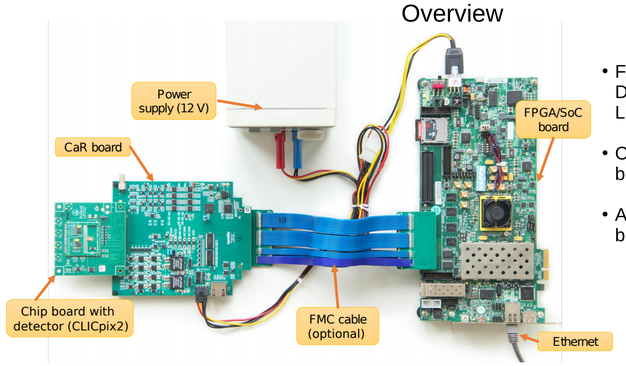
C3PD + CLICpix2

ATLASpix

CLICTD



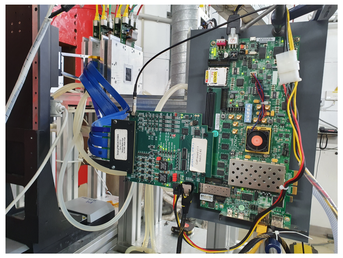
Overview



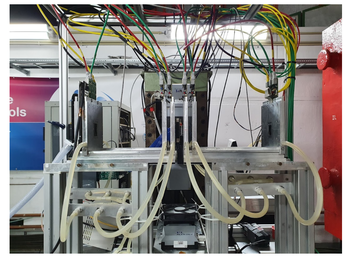
- FPGA/SoC board: Runs DAQ software (Peary) on Linux
- CaR board: interface between FPGA and detector
- Application-specific chip board with detector

Test-beam Integration

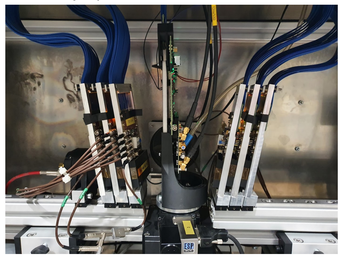
- EUDET telescope at DESY controlled with EUDAQ2 CLICdp Timepix3 telescope at SPS



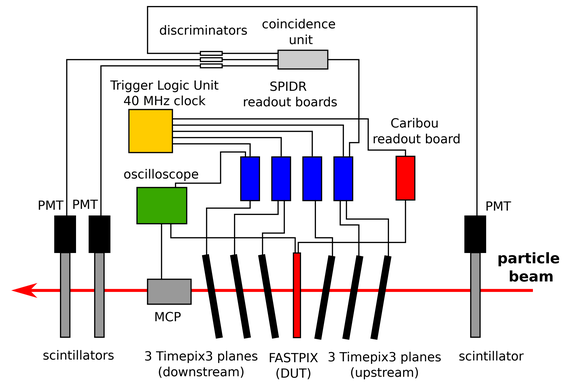
EUDET telescope, CaR and Zynq board



EUDET telescope, side view

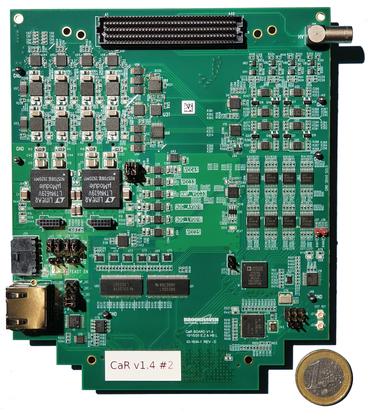


CLICdp Timepix3 telescope with CaR board and DUT



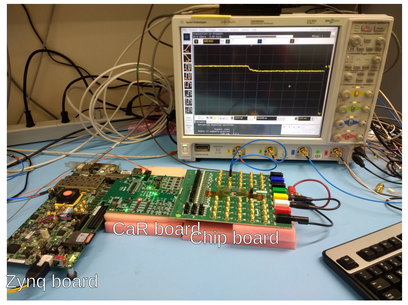
Timepix3 telescope with Caribou and oscilloscope integration

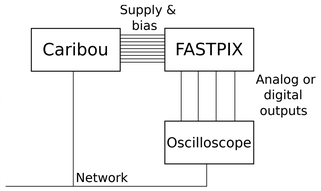
Control and Readout (CaR) board



- **Power**:
  - 8 adjustable power supplies with monitoring (0.8 – 3.6 V, 3A)
- **Analog I/O**:
  - 32 adjustable voltage references (0 – 4 V)
  - 8 adjustable current references (0 – 1 mA)
  - 8 inputs to 12-bit ADC (50 kSPS)
  - 16 inputs to 14-bit ADC (65 MSPS)
  - 4 programmable injection pulsers
- **Digital I/O**:
  - 8 full-duplex high-speed GTx links (<12 Gb/s)
  - 17 LVDS links (bidirectional)
  - 10/14 output and input links, adjustable level (0.8 – 3.6 V)
- **Periphery**:
  - Programmable clock generator, External inputs for high voltage, clock reference, trigger
- **Interfaces**:
  - FMC to FPGA, 320-pin SEARAY to detector

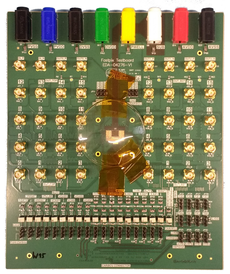
Oscilloscope Integration



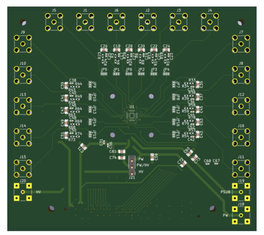


Lab setup with oscilloscope readout via Peary over network (DSO9254A, MSO9404A, and similar)

Recently added chip boards



FASTPIX

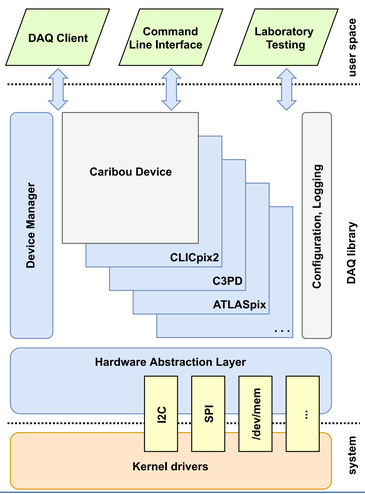


APTS (under development)

Supported devices

- H35Demo/FEI4, ATLASPix, ATLASPix2, ATLASPix3
- CLICTD, CLICpix2/C3PD
- RD50-MPW1, RD50-MPW2
- FASTPIX
- APTS/DPTS (work in progress)

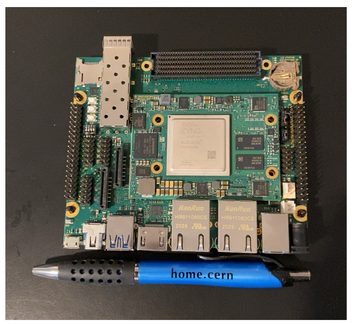
Firmware and Software



- **Firmware**: Based on combination of custom Caribou modules and commercial Xilinx IP cores
  - Provides an interface between CPU (SW) and a detector (HW)
  - Modules are connected to CPU through AXI bus
  - Registers are mapped to CPU memory space (/dev/mem)
- **Software Stack**: Custom **Yocto**-based Linux distribution (meta-caribou)
  - Common Linux tools and packages are pre-installed (ssh, python etc.)
  - Includes Caribou software (EUDAQ, Peary)
- **DAQ Software Framework**: **Peary**
  - Hardware Abstraction Layer (HAL) to handle peripherals as objects in C++
  - Functions to control CaR board, set/measure voltages, capture ADC, ...
  - Various user interfaces: command line, scripting, EUDAQ2 producer for test beam integration

Future Plans

- Reduce size and cost by integrating CaR board with system-on-module
- Upgrade to UltraScale+ Zynq
  - 64 bit platform and increaded CPU performance
- Support for new detectors



Enclustra Mercury+ XU1 SOM on evaluation board

gitlab.cern.ch/Caribou

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