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The Caribou DAQ System –Current Status and Ongoing Developments

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Caribou is a flexible open-source DAQ system designed for laboratory and high-rate beam tests and easy integration of new silicon-pixel detector prototypes. It uses common hardware, firmware and software components that can be shared across different projects, thereby reducing the development effort and cost for such readout systems significantly.

Summary (500 words)

The Caribou flexible readout system consists of a Xilinx Zynq System-on-Chip (SoC) board that runs the Peary DAQ software and detector-specific firmware, and the Control and Readout (CaR) board, which contains programmable power
supplies, current sources, ADCs and DACs, clocks, high- and low-speed communication interfaces, and is connected to an application-specific chip-board that interfaces with the detector.
The CaR board provides the resources used by typical detector prototypes therefore simplifying the detector-specific chip-boards. Data transmission, processing, and detector control is performed by the software and firmware on
the SoC-board and can take advantage of the common components provided by Caribou. Through this versatile hardware and the modular design, the turnaround time for supporting new detectors is minimized.
It can operate standalone and also provides EUDAQ2 integration for operation in test beam environments.

Caribou is developed and maintained as a collaborative effort within the EP R&D silicon work packages of the strategic R&D programme of the CERN Experimental Physics Department (EP R&D) and the RD50 and AIDAinnova collaborations.
Currently 10 participating institutes use the Caribou platform with custom chip boards for 7 types of pixel-detectors, and several more are under development. Caribou is also used for automated testing of calorimeter front-end electronics.

This contribution presents the Caribou system and gives an overview of recent developments, such as a new and improved hardware revision, integration of external waveform sampling, integration of the new ATTRACT FASTPIX chip for
sub-nanosecond timing, and current efforts to migrate the system to the Zynq UltraScale+ platform using a commercial System-on-Module with a custom carrier board.

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