

The new waveform digitizer (DIRAC-V2) for the Mu2e electromagnetic calorimeter at Fermilab

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This paper describes design and performance of the new Digitizer ReAdout Controller of the Mu2e electromagnetic calorimeter, which consists of two 674 CsI crystal annular matrices readout by SiPMs. The 20-channel board performs a 200 MHz sampling of the SiPM signals transmitted by the front-end electronics. The operation in the Mu2e harsh environment, with an expected total ionizing dose of 12krad and neutron fluence of $5 \times 10^{10} \text{ n/cm}^2 @ 1 \text{ MeVeq(Si)/y}$, 1T magnetic field, level of vacuum of 10^{-4} Torr made the design challenging. We report on the board architecture, and design, as well as on the results of the prototype qualification and performance test.

Summary (500 words)

Mu2e aims to measure the ratio of the rate of the neutrino-less muon to electron coherent conversion in the field of an aluminum nucleus relative to the rate of ordinary muon capture. Mu2e will exploit an intense pulsed muon beam and a detector system where the primary components employed to search for the monoenergetic 105 MeV conversion electron signal are the straw tracker and the electromagnetic calorimeter. The calorimeter provides an additional rejection factor of 200 on cosmic muons, a tracker independent trigger and improve pattern recognition quality and efficiency for the electron tracks. The expected calorimeter performance are $\sigma_{E/E} < 10\%$, $\sigma(t) < 500 \text{ ps}$ and a position resolution $< 1 \text{ cm}$. The calorimeter employs 1348 undoped CsI crystals, arranged in two annular matrices (disks) located inside the detector cryostat. Each crystal is coupled to two SiPMs arrays connected to the Front End Electronics. A mezzanine board controls a group of 20 Amp-HV chips. Groups of 20 differential signals are sent to the Digitizer ReAdout Controller board (DIRAC-V2). To limit the number of pass-through connectors and the length of the cables, the readout and digitization electronics will be located inside the cryostat. This choice has made the DIRAC-V2 design challenging due to the harsh operational environment: neutron fluence $5 \times 10^{10} \text{ n/cm}^2 @ 1 \text{ MeVeq(Si)/y}$, TID 12 krad, 1T magnetic field, which have required an extended campaign of tests to qualify the employed electronic components, and a level of vacuum of 10^{-4} Torr, which has required the design of a dedicated cooling system for power dissipation. The DIRAC-V2 is an evolution of the DIRAC-V1 and the improvements derive from the qualification campaign and performance tests carried out on DIRAC-V1. The DIRAC-V2 core is a large FPGA (Polarfire MPF300) with configuration cells immune to Single Event Upset. Data coming from 10 ultralow-power double channels 12-bit 250 MHz ADCs (ADS4229) are handled by the FPGA. Sparsified and compressed data form packets that are optically transmitted through a fiber transceiver (VTRx) to the Mu2e event builder using a custom protocol. The board was required to pass different qualification tests: Total Ionizing Dose up to 12 krad, Single Event Upset, Neutron Displacement Test and magnetic field. An ultra-low noise jitter cleaner (LMK04828) provides a high-performance clock to the FPGA and ADCs, with the option to fine tune relative phases with an accuracy up to 100 ps. The power distribution is handled by 3 DC-DC converters (LMZM33606) and 6 LDO (MIC69502) to provide rails to the analog components. The DIRAC-V2 board follows a custom form factor (233 mm x 165 mm x 2.127 mm), realized in FR408-HR, and relevant lines controlled impedance. To validate the DIRAC-V2 analog section in terms of dynamic, SNR, bandwidth, and linearity, we assembled a full system chain (one CsI crystal, two FEE board, one mezzanine board and the DIRAC-V2 prototype) for a cosmic ray test. The test demonstrated that the DIRAC-V2 analog section performs satisfactorily: the signals shapes are as expected from the Monte Carlo simulation, and the time resolution is 350 ps

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