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The Fast Beam Condition Monitor as a standalone luminometer of the CMS experiment at the HL-LHC

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In the Phase-2 CMS upgrade, a luminosity uncertainty of 1% is targeted. To achieve this goal, measurements from multiple luminometers with orthogonal systematics are required. A standalone luminometer, the Fast Beam Condition Monitor (FBCM) is being designed for online bunch-by-bunch luminosity measurement. Its fast timing properties also enable the measurement of beam induced background. In this talk, the hardware architecture and the read-out protocol of the FBCM is described. The expected performance with a simple behavioral model of the front-end comprising a constant fraction discriminator is discussed, though the final implementation in the ASIC is still under discussion.

Summary (500 words)

A fast beam condition monitor (FBCM) is being designed as a standalone luminometer to run independently of the CMS central trigger and data acquisition systems at the HL-LHC and to provide bunch-by-bunch luminosity measurement in real time. The ultimate goal of 1% luminosity uncertainty after final calibration implies a deviation from linearity of less than 0.02%/(Hz/μb). To meet this goal, the FBCM will utilize silicon-pad sensors with a zero-counting algorithm of the observed hits and it will provide the time of arrival (ToA) and the time over threshold (ToT) of the signal pulse with a few ns resolution. The FBCM will have a semi-digital readout to transfer these data to the back-end, with the front-end chip producing a non-clocked output pulse upon the creation of an ionising signal in the silicon-pad sensor.
The lpGBT (Low Power GigaBit Transceiver, an ASIC widely used for data transmission and control in the Phase-2 projects) will receive the semi-digital output i.e. called e-links via flex cables. It will continuously sample the front-end output pulse every 0.78 ns corresponding to the e-link speed (1.28 Gbps), then transmit it to the back-end over an optical transceiver, the VTRx+. At the back-end, an ATCA (Advanced Telecommunications Computing Architecture) digital processing unit finds the rising edge and pulse duration and tags the ToA and the ToT, respectively, after synchronizing to the LHC clock. The ATCA unit histograms the number of hits per bunch-crossing per sensor. The probability of zero-hit occurrence and the mean number of hits – assuming a Poisson distribution for the hits – are computed from these histograms. The timing information provides the capability to measure beam-induced background, as well. To optimize resources, the FBCM ASIC design will be launched in early 2022, and make the most use of existing 65 nm blocks, optimized for the functionality and performance of FBCM.
In this talk, the expected performance of the FBCM with a simple front-end behavioral model is presented. The model includes a fast analog amplifier with 14 ns settling time from peak to baseline, shapers and a constant fraction discriminator (CFD) with the capability of adjusting the thresholds to tune the rising edge to the signal peak. The rising edge of the front-end output pulse corresponds to the peak of the amplified analog signal (using 2 ns and 0.51 for the CFD delay and the fraction, respectively) and the pulse duration is equivalent to the ToT. The pulse width of the semi-digital output is a monotonic function of the signal amplitude, which is also beneficial to monitor the MIP amplitude spectrum and thus the sensor's radiation damage.
Simulation results also show that the FBCM will provide the required statistical uncertainty and deviation from linearity by employing 336 silicon-pad sensors, each with an area of about 3 mmˆ2. In addition, the front-end with sensitivity to at least 6000 electrons will satisfy the longevity constraints for an exposure of 1 MeV neutron equivalent fluence of 3.5×10ˆ{15} per cmˆ2.

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